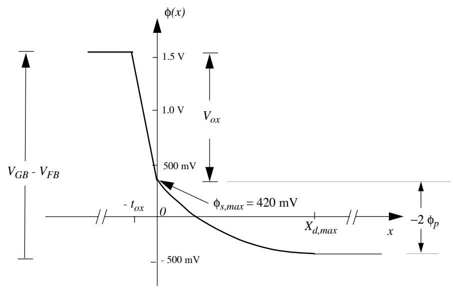
The Inverted MOS Capacitor ($V_{GB} > V_{Tn}$)

- We consider the surface potential as fixed ("pinned") at $\phi_{s,max}$ = - 2 ϕ_p



- What is the inversion charge Q_N?

  see Section 3.7 for the derivation

  consider: bulk charge is constant for $V_{GB} > V_{Tn}$ --> all of the additional charge in the silicon is stored in the inversion layer, once inversion occurs. The inversion layer is separated from the gate by the gate oxide; we can relate the inversion charge (per cm^2) to the applied voltage over V_{Tn} through C_{ox} the capacitance (per cm^2) of the oxide

$$Q_N = -C_{ox}(V_{GB} - V_{Tn})$$

Charge Storage in the MOS Structure

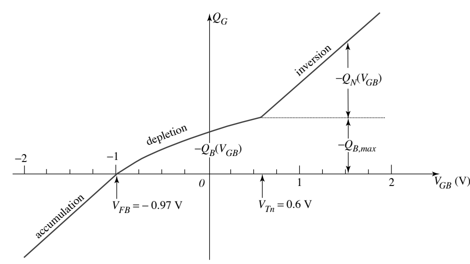
- Three regions of operation:

  Accumulation: $q_G = C_{ox}$ (v_{GB} - v_{FB}) ... parallel plate capacitor

  Depletion: q_G = - $q_B(v_{GB})$, with the bulk (depletion) charge in the silicon being a nonlinear function of v_{GB}

  Inversion: q_G = - q_N - $q_{B,max}$, where $q_{B,max} = q_B(v_{GB} = V_T)$ is the depletion charge at the onset of inversion and

- Sketch of the gate charge as a function of gate-bulk voltage:

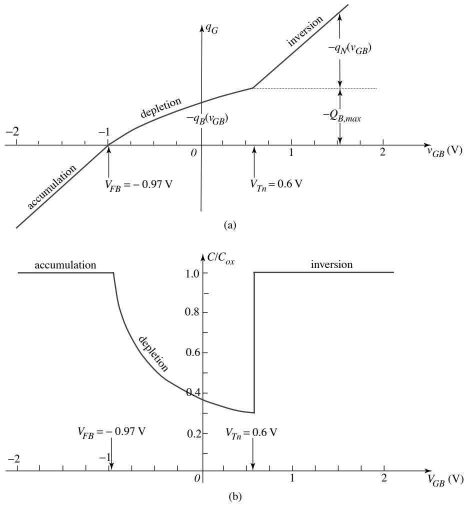


MOS Capacitance

- The capacitance of the MOS structure is defined as

$$C = \left.\frac{dq_G}{dv_{GB}}\right|_{V_{GB}}$$

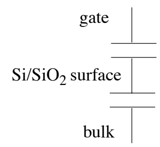
- From sketch, determine the slope and plot as the capacitance



Physical Interpretation of MOS Capacitance

- ***Accumulation***: parallel plate capacitor --> $C = C_{ox}$

- ***Depletion***: increment in gate charge is mirrored at bottom of depletion region, so capacitance model is C_{ox} in series with the depletion region capacitance C_b



$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

$$C_b = \frac{\varepsilon_s}{X_d}$$

Note that X_d is a function of V_{GB}

$$C = C_{ox} || C_b$$

- ***Inversion***: bulk charge is no longer changing with V_{GB} --> an increment in gate charge is mirrored in the inversion layer under the gate.

  The capacitance is therefore the same as in accumulation --> $C = C_{ox}$

Understanding MOS Capacitors

- **Step 1**: identify the flatband voltage from the gate and bulk potentials in equilibrium
- **Step 2**: determine whether $V_{GB} > V_{FB}$ leads to *accumulation* or to *depletion*

  substrate is n-type --> accumulation   substrate is p-type --> depletion

  Why? positive charge on gate (since V_{GB} - $V_{FB} > 0$ V) *must* be mirrored by a *negative* charge in the substrate.

  n-type substrate: negatively charged electrons are accumulated under the gate
  p-type substrate: negatively charged ionized acceptors are left, after holes are repelled away from positive charge on gate
- **Step 3**: construct $C(V_{GB})$ plot, using the knowledge that the substrate is depleted on the other side of V_{FB} from accumulation in Step 2 and that *inversion* occurs after depletion. Calculation of V_T and C_{min} is necessary to quantify the plot
- Additional data point: determine state of MOS structure in thermal equilibrium ($V_{GB} = 0$ V) ... accumulation or [depletion/inversion]

Example:

gate: p^+ polysilicon (where ϕ_{p+} = - 550 mV); gate oxide thickness = 200 Å ,
substrate: n type silicon, ϕ_n = 480 mV ($N_d = 10^{18}$ cm^{-3})

V_{FB} = - (-550 mV - 480 mV) = + 1.03 V

V_{GB} - $V_{FB} > 0$ V --> accumulated; substrate is depleted for $V_{GB} < 1.03$ V

Check: $V_{GB} = 0$ --> negative charge on gate; positive in bulk (since gate is at - 0.55 V and substrate is at + 0.48 V in thermal equilibrium) --> positive donors in depletion region under gate ... and possibly holes due to inversion

MOS Capacitance-Voltage Curve

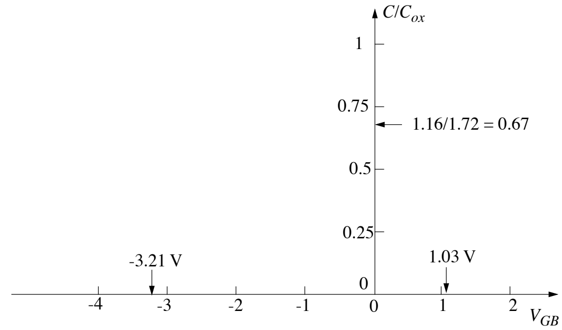
- Evaluate threshold voltage V_{Tp}

$$V_{Tp} = V_{FB} - 2\phi_n - \frac{\sqrt{2q\varepsilon_s N_d (2\phi_n)}}{C_{ox}} = 1.03 - 2(0.48) - 3.28 = -3.21 \text{ V}$$

- Minimum capacitance occurs just prior to inversion and is the series combination of the oxide capacitance and the maximum depletion capacitance:

$$C_{min} = \left(\frac{\varepsilon_{ox}}{t_{ox}}\right) \| \left(\frac{\varepsilon_s}{X_{d,\,max}}\right) = \left(\frac{3.45\times10^{-13}}{2\times10^{-6}}\right) \| \left(\frac{1.04\times10^{-12}}{2.9\times10^{-6}}\right) = 1.16 \text{ fF/cm}^2$$

- Maximum capacitance is C_{ox} = 1.72 fF/cm^2.



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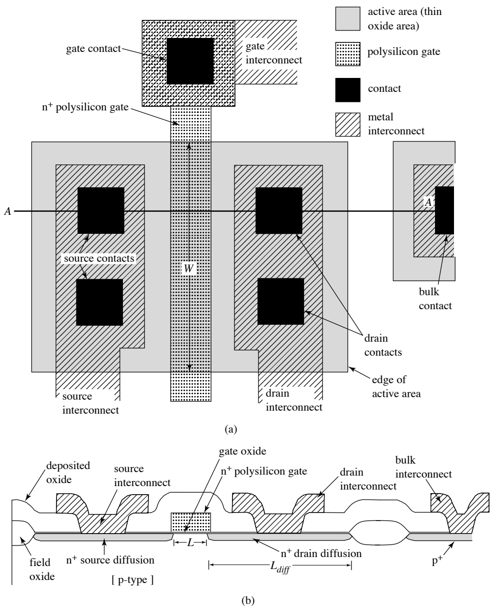
MOS Field Effect Transistors

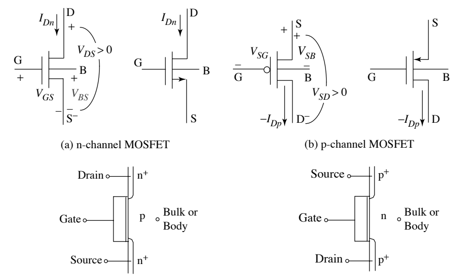


MOSFET Circuit Symbols

Two complementary devices (each with two symbols): both are very useful

p-substrate (n-type channel under gate oxide)

n-substrate (p-type channel under gate oxide)



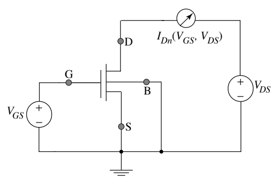
Four electrical terminals: source (lowest potential for n-channel, highest for p-channel), drain, gate, and bulk.

Basic concept: inversion layer (called the channel) formed under gate between source and drain enables drift current

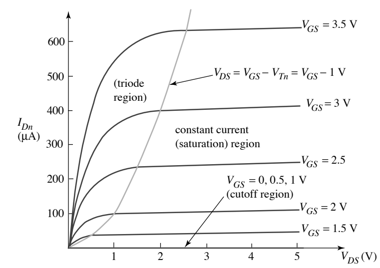
n-Channel MOSFET Drain Characteristics

Set-up: $I_G = 0$, $V_{DB} = V_{DS} > 0$ to reverse-bias pn junctions to bulk.

- Measurement scheme: short bulk to source to make it a three terminal device, vary gate voltage, drain voltage and see effect on drain current.



(a)

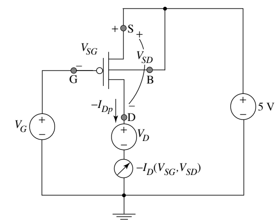


(b)

p-Channel MOSFET Drain Characteristics

Set-up: $I_G = 0$, $V_{BD} = V_{SD} > 0$ to reverse-bias pn junctions to bulk.

- Measurement scheme: short bulk to source to make it a three terminal device, vary gate voltage, drain voltage and see effect on drain current $-I_D$



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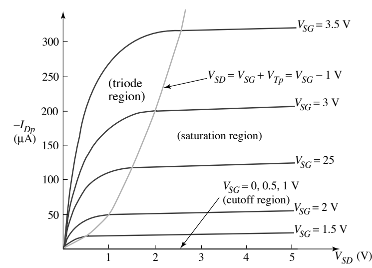

(b)

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