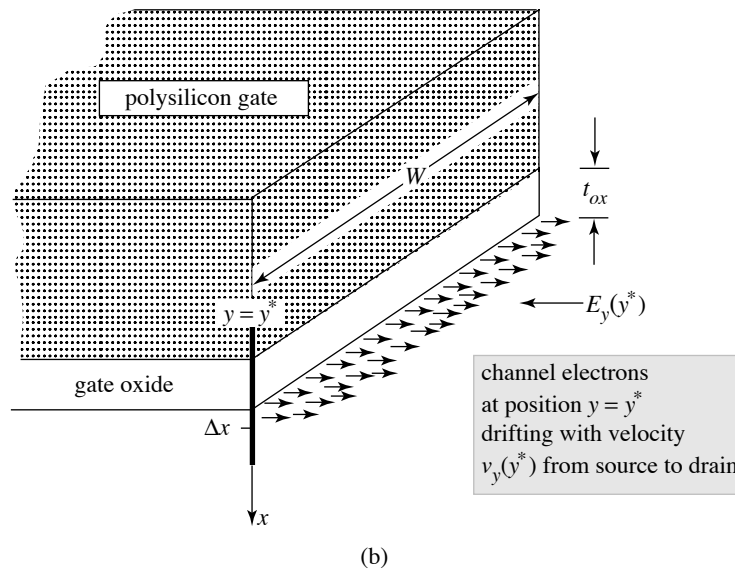
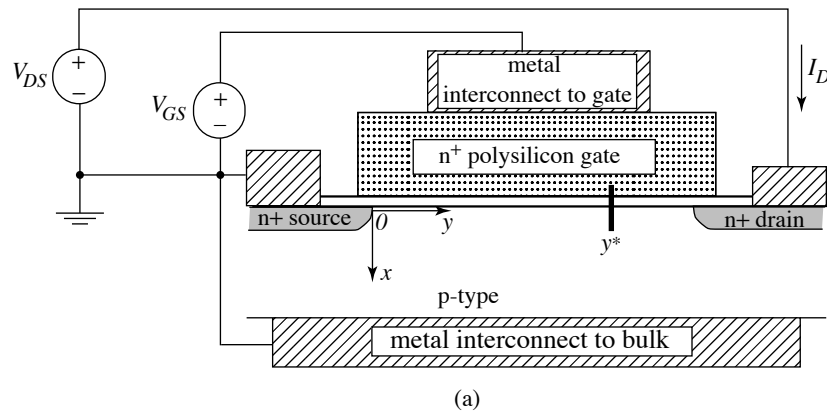


# Quantitative MOSFET

- **Step 1.** Connect the MOS capacitor results for the electron charge in the inversion layer  $Q_N$  to the drain current.



## Drift Current Equation

- Drift current for electrons in the channel:

$$J_y(x, y) = -qn(x, y)v_y(y)$$

The drain current at position  $y$  is the integral of the drift current density across the cross section. Since the conventional direction of  $I_D$  is *opposite* to the direction of the  $y$  axis, we insert a minus sign:

$$I_D = -W \int_0^{\Delta x} J_y(x, y) dx = Wv_y(y) \left( \int_0^{\Delta x} qn(x, y) dx \right)$$

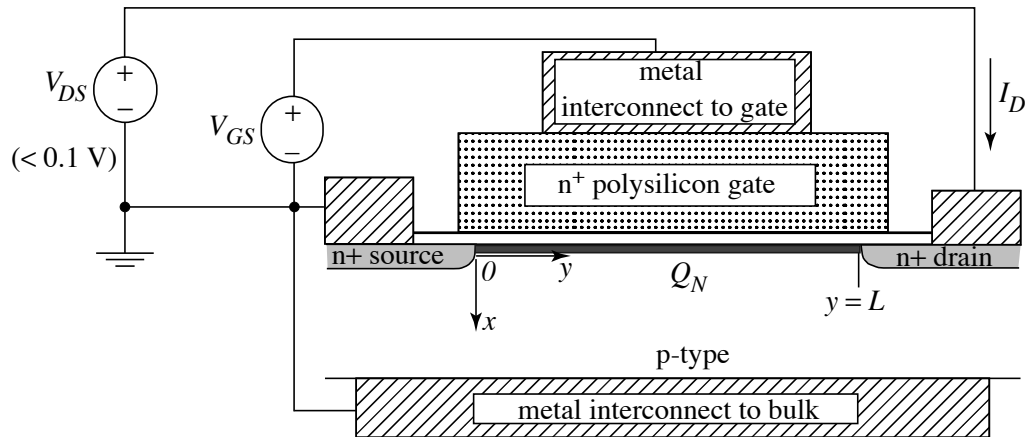
- The integral is the negative of the electron charge in the channel, per unit area, at point  $y$ . The symbol for this quantity is  $-Q_N(y)$ :

$$I_D = -Wv_y(y)Q_N(y)$$

Note that  $I_D$  isn't a function of the position in the channel

## MOSFET DC Model: a First Pass

- Start simple -- small  $V_{DS}$  makes the channel uniform



- Channel charge: MOS capacitor in inversion, with  $V_{GB} = V_{GS}$ .

$$Q_N = -C_{ox}(V_{GB} - V_{Tn}) = -C_{ox}(V_{GS} - V_{Tn})$$

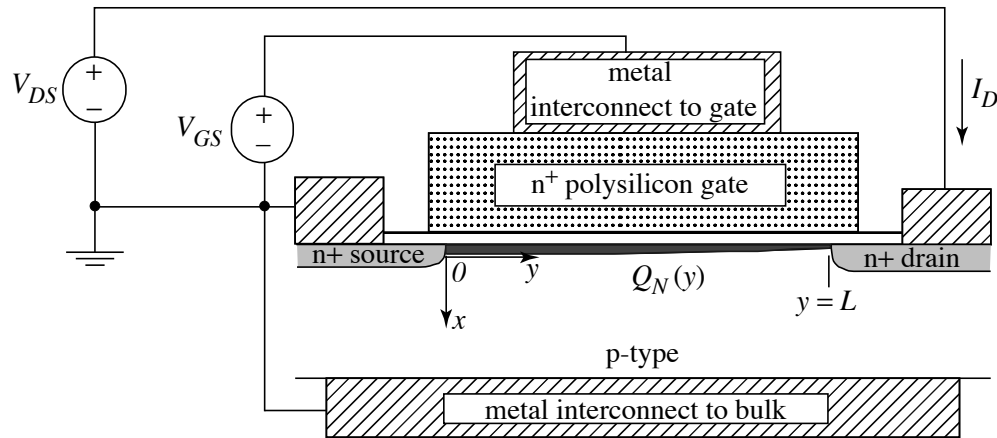
- Drift velocity: electric field is just  $E_y = -V_{DS}/L$  so  $v_y = -\mu_n(-V_{DS}/L)$
- Drain current equation for  $V_{DS}$  “small” ... say, less than 0.1 V.

$$I_D = \mu_n C_{ox} \left( \frac{W}{L} \right) (V_{GS} - V_{Tn}) V_{DS}$$

Note that  $I_D$  is proportional to  $V_{DS}$  with channel resistance under gate control. This voltage controlled resistor region is sometimes useful.

## Triode Region

- Increase  $V_{DS}$  -- channel charge becomes a function of position  $y$ .



- First pass: approximate the drain current equation by taking averages of the channel charge and the drift velocity (Second pass: Section 4.4 (not assigned))

$$I_D \approx -W \overline{Q_N} \overline{v_y}$$

- Average drift velocity: still use  $\mu_n (V_{DS} / L)$  -- which is a very rough approximation.

## Triode Region (Cont.)

- Next, approximate the average channel charge by averaging  $Q_N(y=0)$  at the source end and  $Q_N(y=L)$  at the drain end of the channel:

$$Q_N(y=0) = -C_{ox}(V_{GS} - V_{Tn})$$

At the drain end, the positive drain voltage *reduces* the magnitude of the channel charge ... why? The effect can be approximated by using  $V_{GD}$  (the drop from drain to channel, at  $y = L$ ) --

$$Q_N(y=L) = -C_{ox}(V_{GD} - V_{Tn}) = -C_{ox}(V_{GS} - V_{DS} - V_{Tn})$$

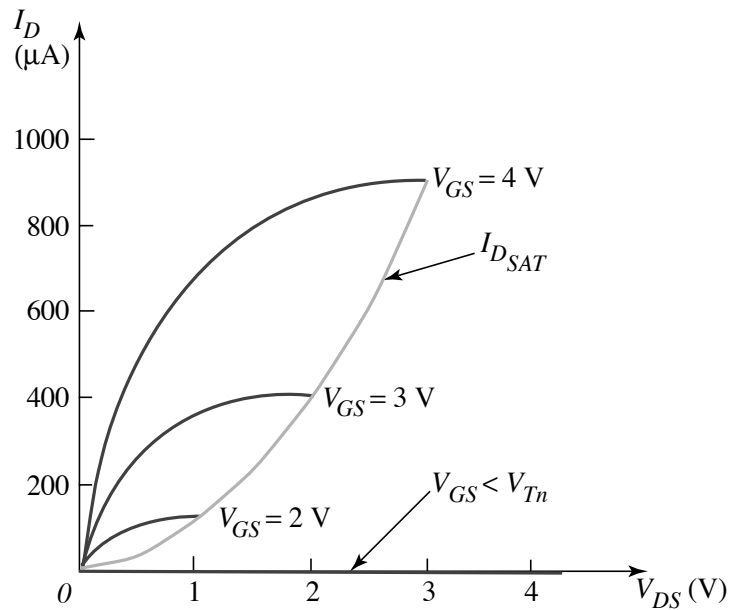
Note that  $V_{GD} = V_{GS} - V_{DS} > V_{Tn}$  in order for there to be a channel left at the drain end.

- Substituting, we derive the equation for the triode region, which is defined by  $V_{GS} - V_{DS} > V_{Tn}$  and  $V_{GS} > V_{Tn}$ .

$$I_D = \mu_n C_{ox} \left( \frac{W}{L} \right) (V_{GS} - V_{Tn} - V_{DS}/2) V_{DS}$$

## Drain Characteristics

- Example:  $\mu_n C_{ox} (W/L) = 50 \mu\text{A}/\text{V}^2$ ,  $V_{Tn} = 1 \text{ V}$ , and  $(W/L) = 4$ .



- What happens when  $V_{DS} > V_{GS} - V_{Tn} = V_{DS(sat)}$ ?  $|Q_N(y=L)| = 0$ !

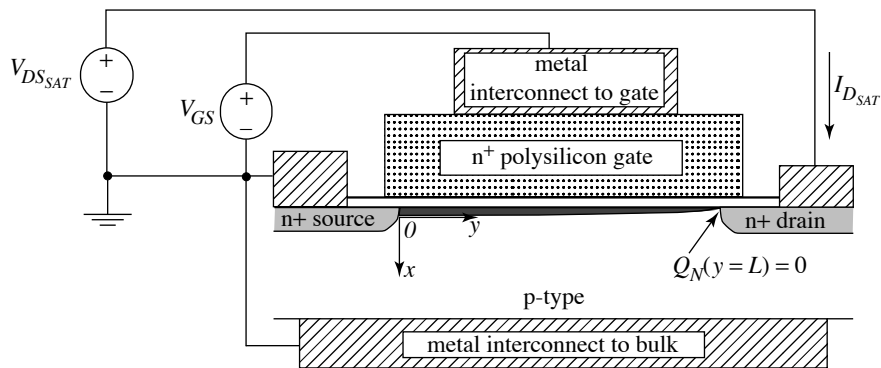
Initial thought is that the lack of a channel at the drain end means that  $I_D$  must drop to zero ... **WRONG!**

Drain terminal loses control over channel --> drain current “saturates” and remains constant (to first approximation) at the value given by  $V_{DS} = V_{DS(sat)}$ .

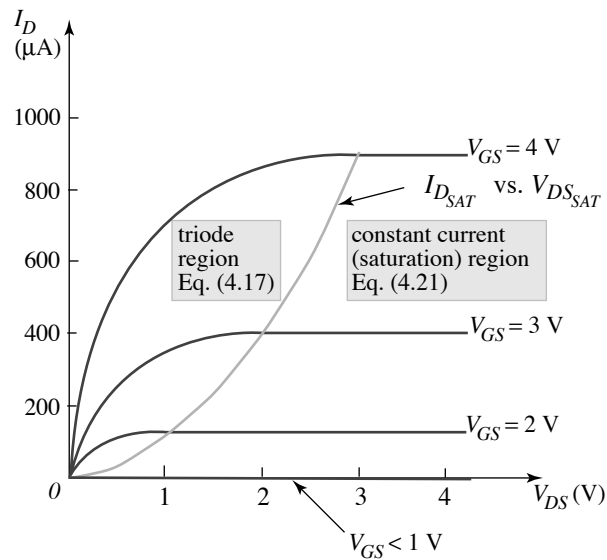
# Saturation Region

- When  $V_{GS} > V_{Tn}$  and  $V_{DS} > V_{DS(sat)} = V_{GS} - V_{Tn}$ , the drain current is:

$$I_D = I_{D(sat)} = \mu_n C_{ox} \left( \frac{W}{2L} \right) (V_{GS} - V_{Tn})^2$$



- Full model:



## MOSFET Circuit Models

- n-channel MOSFET drain current in cutoff, triode, and saturation:

$$\begin{aligned} I_D &= 0 \text{ A} && (V_{GS} \leq V_{Tn}) \\ I_D &= \mu_n C_{ox} (W/L) [V_{GS} - V_{Tn} - (V_{DS}/2)] (1 + \lambda_n V_{DS}) V_{DS} && (V_{GS} \geq V_{Tn}, V_{DS} \leq V_{GS} - V_{Tn}) \\ I_D &= \mu_n C_{ox} (W/(2L)) (V_{GS} - V_{Tn})^2 (1 + \lambda_n V_{DS}) && (V_{GS} \geq V_{Tn}, V_{DS} \geq V_{GS} - V_{Tn}) \end{aligned}$$

Numerical values:

$\mu_n$  is a function of  $V_{GS}$  along the channel and is much less than the mobility in the bulk (typical value  $215 \text{ cm}^2/(\text{Vs})$ ) -- therefore, we consider that  $\mu_n C_{ox}$  is a measured parameter. Typical value:  $\mu_n C_{ox} = 50 \mu\text{AV}^{-2}$

$\lambda_n$ , sometimes called the channel length modulation parameter, increases as the channel length  $L$  is reduced:

$$\lambda_n \approx \frac{0.1 \mu\text{mV}^{-1}}{L}$$

The triode region  $I_D$  equation has  $(1 + \lambda_n V_{DS})$  added in order to avoid a jump at the boundary with the saturation region. For hand calculation of DC voltages and currents, this term is usually omitted from  $I_D$ .

$V_{Tn}$  = threshold voltage = 0.7 - 1.0 V typically for an n-channel MOSFET.

## Backgate Effect

- The threshold voltage is a function of the bulk-to-source voltage  $V_{BS}$  through the *backgate effect*.

$$V_{Tn} = V_{TO_n} + \gamma_n (\sqrt{-V_{BS} - 2\phi_p} - \sqrt{-2\phi_p})$$

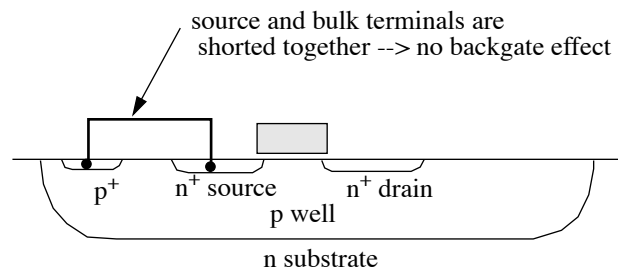
where  $V_{TO}$  is the threshold voltage with  $V_{BS} = 0$  and  $\gamma$  is the backgate effect parameter

$$\gamma_n = (\sqrt{2q\epsilon_s N_a}) / C_{ox}$$

- Physical origin:  $V_{BS}$  (a negative voltage to avoid forward biasing the bulk-to-source pn junction) increases the depletion width, which increases the bulk charge and thus, the threshold voltage.

$$I_D = I_D(V_{GS}, V_{DS}, V_{BS}) \text{ since } V_{Tn} = V_{Tn}(V_{BS})$$

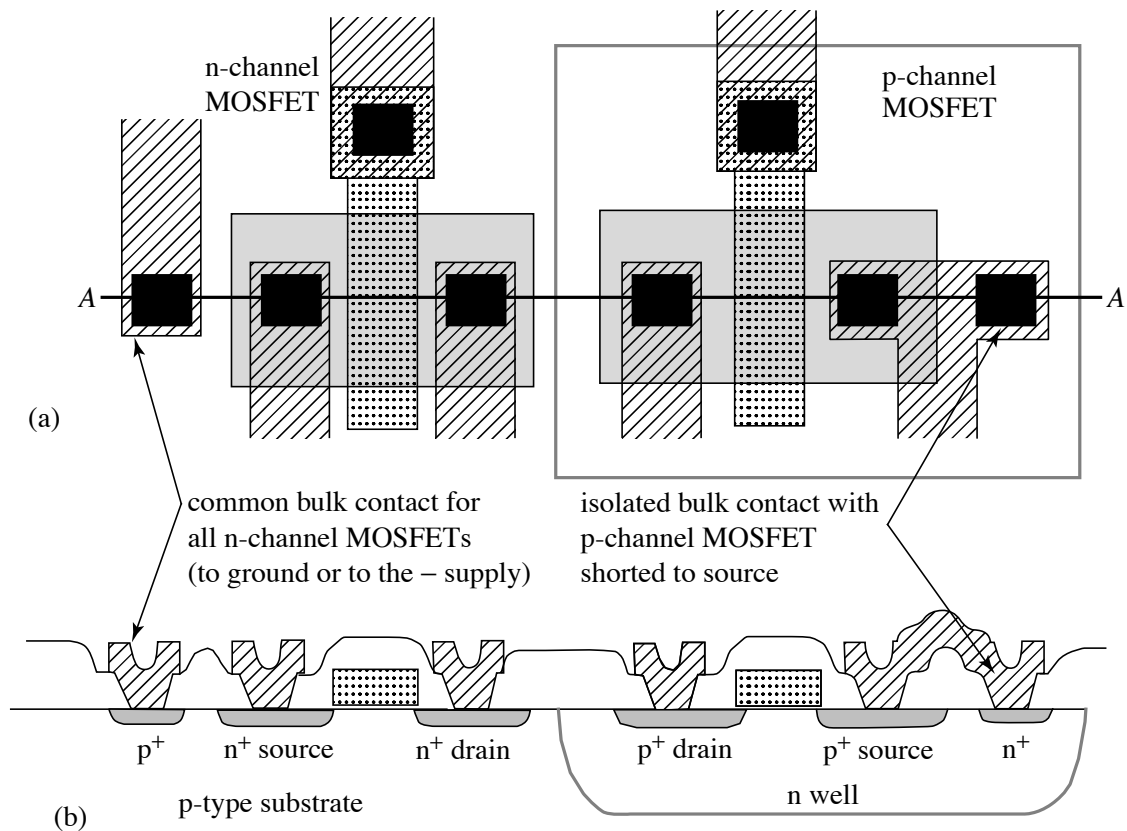
Common situation is that  $V_{BS} = 0$  by electrically shorting the source to the bulk (either the substrate or a deep diffused region called a *well*)



For this case,  $V_{Tn} = V_{TO_n}$ .

## p-channel MOSFETs

- Structure is *complementary* to the n-channel MOSFET
- In a CMOS technology, one or the other type of MOSFET is built into a *well* -- a deep diffused region -- so that there are electrically isolated “bulk” regions in the same substrate



## p-channel MOSFET Models

- DC drain current in the three operating regions:  $-I_D > 0$

$$\begin{aligned}
 -I_D &= 0 \text{ A} && (V_{SG} \leq -V_T) \\
 -I_D &= \mu_p C_{ox} (W/L) [V_{SG} + V_{Tp} - (V_{SD}/2)] (1 + \lambda_p V_{SD}) V_{SD} && (V_{SG} \geq -V_{Tp}, V_{SD} \leq V_{SG} + V_{Tp}) \\
 -I_D &= \mu_p C_{ox} (W/(2L)) (V_{SG} + V_{Tp})^2 (1 + \lambda_p V_{SD}) && (V_{SG} \geq -V_{Tp}, V_{SD} \geq V_{SG} + V_{Tp})
 \end{aligned}$$

- The threshold voltage with backgate effect is given by:

$$V_{Tp} = V_{TOp} - \gamma_p ((\sqrt{-V_{SB} + 2\phi_n}) - \sqrt{2\phi_n})$$

Numerical values:

$\mu_p C_{ox}$  is a measured parameter. Typical value:  $\mu_p C_{ox} = 25 \mu\text{AV}^{-2}$

$$\lambda_p \approx \frac{0.1 \mu\text{mV}^{-1}}{L}$$

$V_{Tp} = -0.7$  to  $-1.0$  V, which should be approximately  $-V_{Tn}$  for a well-controlled CMOS process