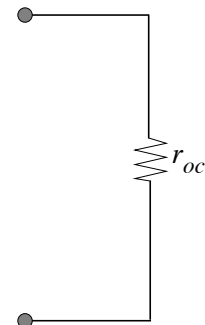
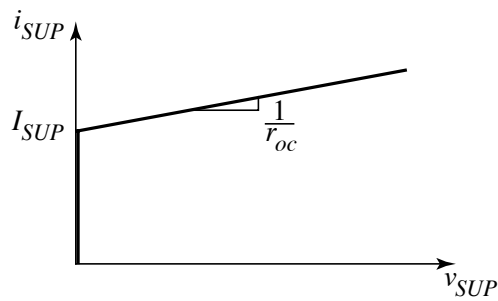
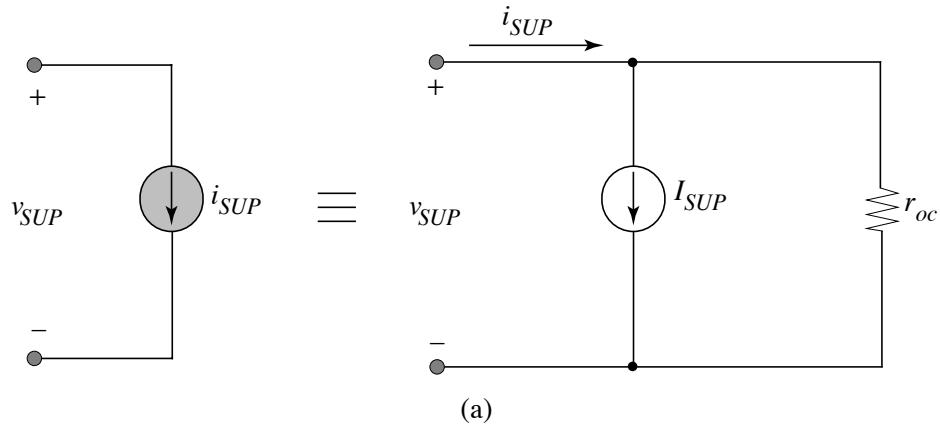


## Current-Source Pull-Up

- What else could be connected between the drain and  $V_{DD}$ ?

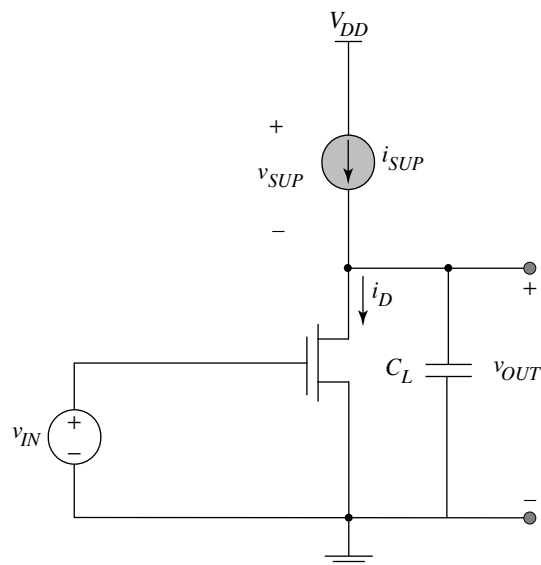


Resistor can be quite large --> can get high small-signal gain (and therefore, a narrow transition region)

DC Current is large --> fast transitions

## MOS Inverter with Current-Source Pull-Up

- Replace resistor with current source



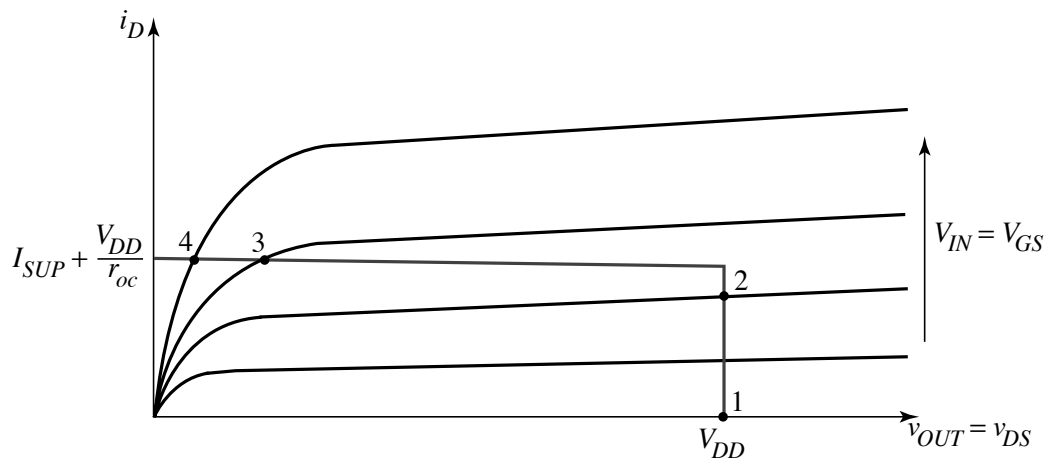
- Find the voltage transfer curve graphically by superimposing  $i_{SUP}$  vs.  $v_{OUT}$  (load line) on top of the drain characteristics

we have a plot of  $i_{SUP}$  vs.  $v_{SUP}$  and we know that  $v_{OUT} = V_{DD} - v_{SUP}$

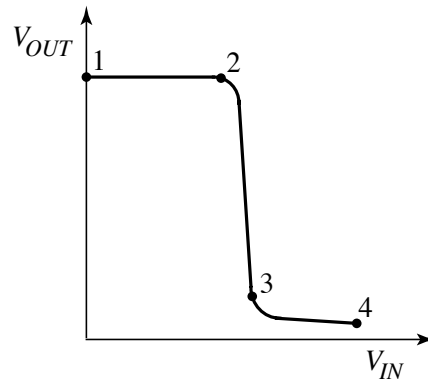
therefore, the current source  $i_{SUP}$  vs.  $v_{OUT}$  is a “mirrored” version of the plot of  $i_{SUP}$  vs.  $v_{SUP}$

## Load-Line Analysis of Improved Inverter

- Voltage transfer curve with idealized current-source pull-up is much closer to that of the ideal inverter



(a)



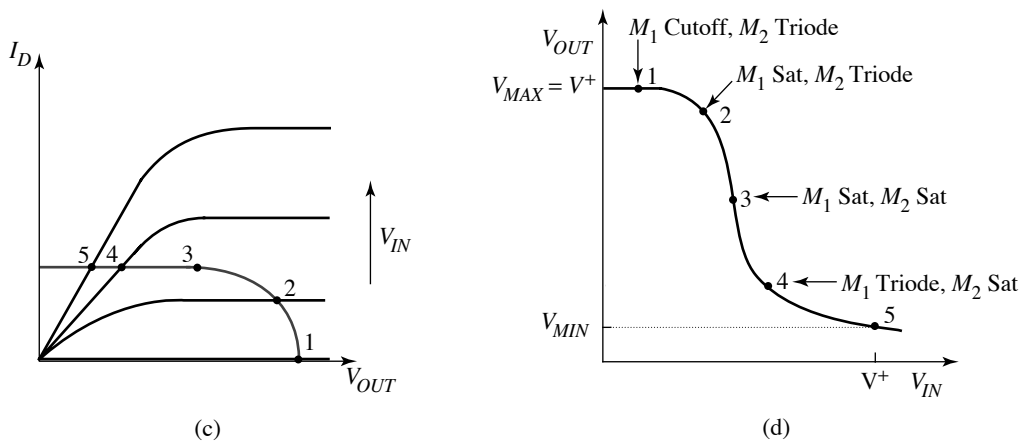
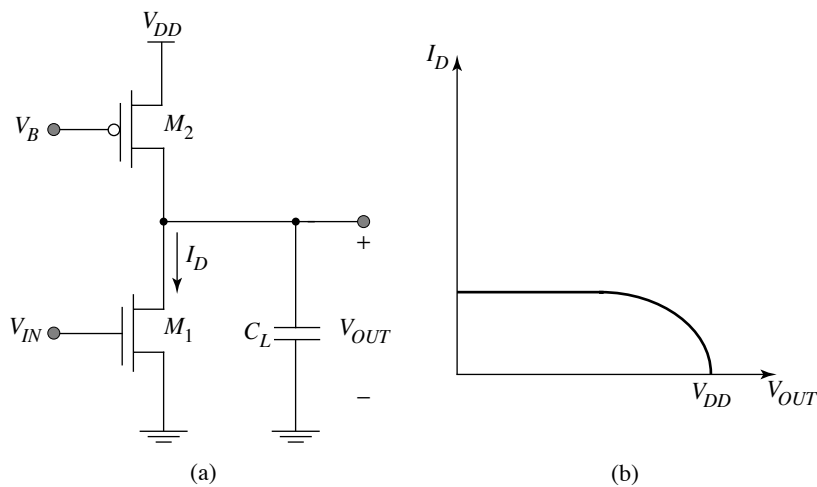
(b)

- Question: how to implement the current source using transistors?

## p-channel MOSFET as a Current-Source Pull-Up

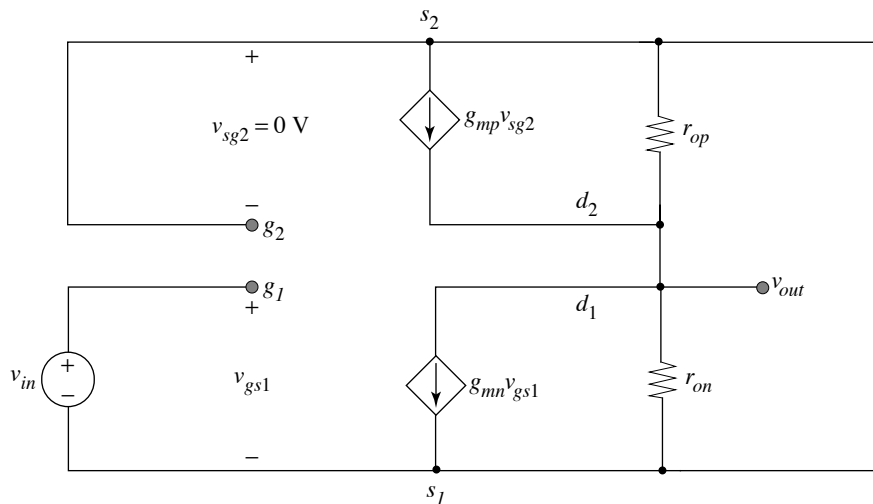
- Use p-channel MOSFET  $M_2$  (with well connected to the source to make  $V_{SB} = 0$  and source connected to the supply voltage)

connect the gate to a battery  $V_B$  that results in an “appropriate” value of DC current  $-I_{D2} = I_{D1}$ .



## Voltage Transfer Curve

- In order to find the slope at  $V_{IN} = V_M$ , we note that both transistors are saturated there (near point 3) and that the small-signal models from Chapter 4 are valid



- Slope of transfer curve at  $V_{IN} = V_M$ :

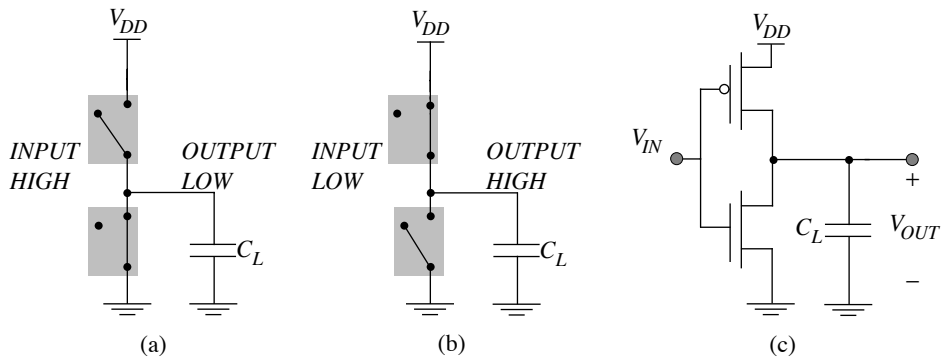
$$\left. \frac{dv_{OUT}}{dv_{IN}} \right|_{V_M} = \frac{v_{out}}{v_{in}} = -g_{mn}(r_{on} || r_{op})$$

The transition region can be *much* steeper than for the resistor load, while the large DC drain current at  $V_M$  results in short propagation delays ... what more could be desired?

- DC power is wasted when inverter is in  $V_{OUT} = V_{MIN}$  state ... need a “switchable” current supply to disconnect  $V_{DD}$  when output is low

## Complementary MOS (CMOS) Inverter

- Concept: transistor switches connect output either to  $V_{DD}$  or to ground



- Practical realization: connect input to gate of p-channel device.

$$V_{IN} = V_{DD} \rightarrow V_{SG2} = V_{DD} - V_{IN} = 0 < -V_{Tp} \rightarrow \text{cutoff}$$

$$V_{IN} = 0 \rightarrow V_{SG2} = V_{DD} - V_{IN} = V_{DD} \gg -V_{Tp} \rightarrow \text{on (triode region)}$$

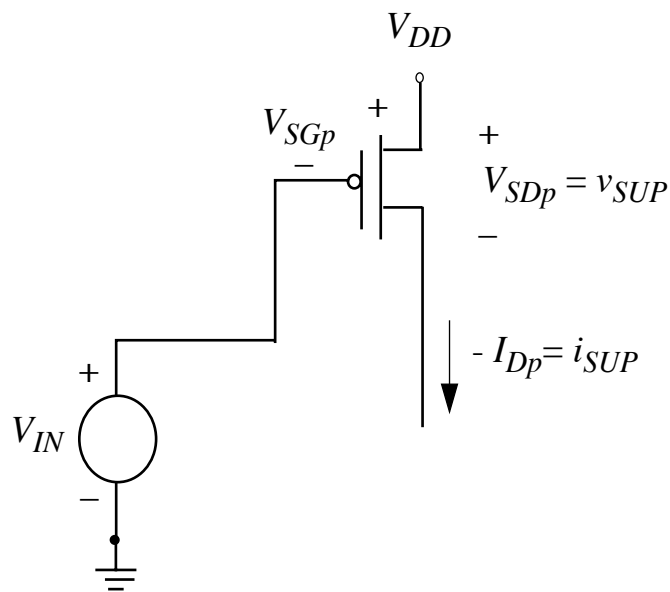
- Graphical analysis: need to find *family* of load lines since input is connected to gate of  $M_2$

## p-Channel MOSFET Characteristics

- p-channel MOS load device:

$$V_{SGp} = V_{DD} - V_{IN}$$

as  $V_{IN}$  increases, the source-gate voltage  $V_{SGp}$  decreases.



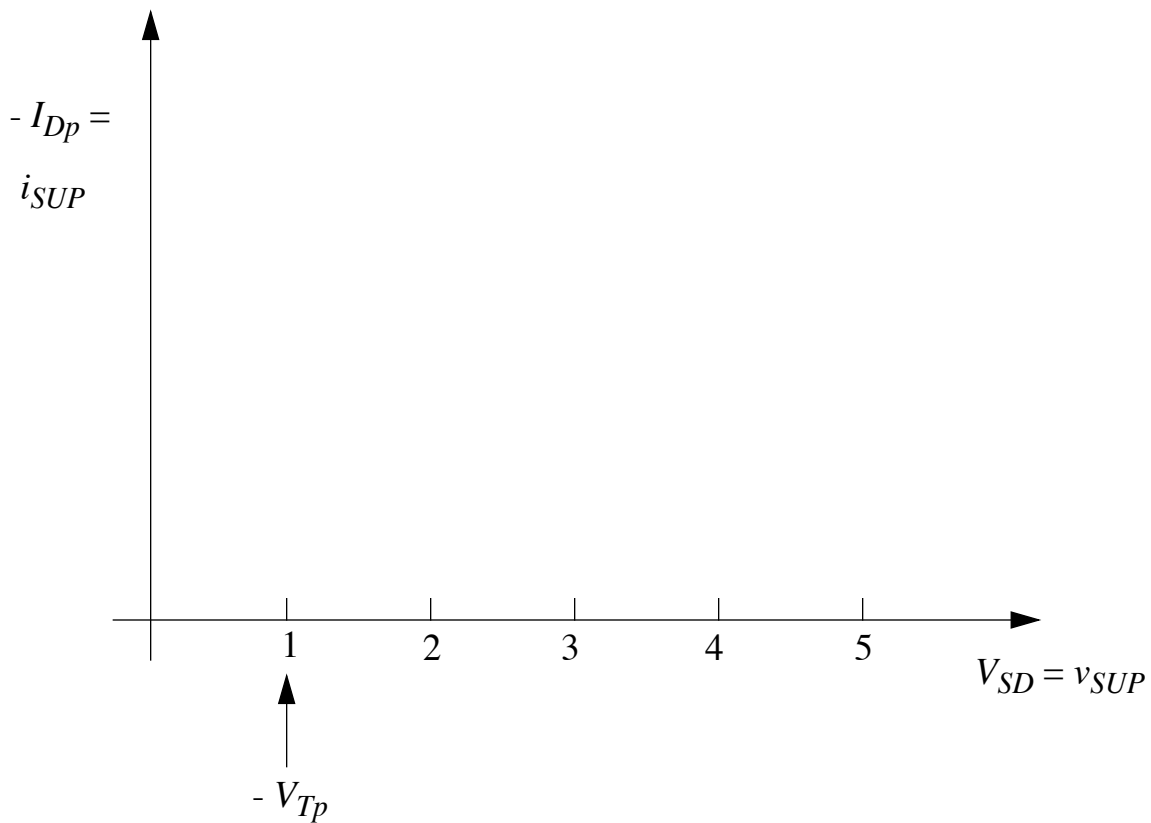
note that the bulk connection is tied to the source ( $V_{DD}$ ), which results in a constant threshold voltage.

## Switchable Current-Source Pull-Up

\* The drain characteristics are  $-I_{Dp} = -I_{Dp}(V_{SG}, V_{SD})$ , which can be expressed as the “switchable” pull-up’s current-voltage characteristic,

$$i_{SUP} = i_{SUP}(V_{IN}, v_{SUP})$$

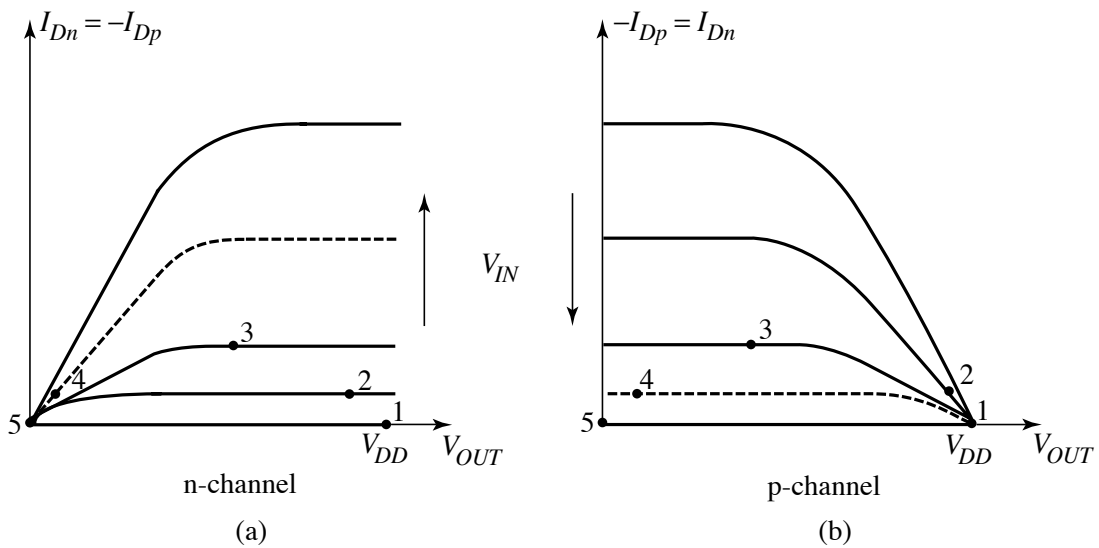
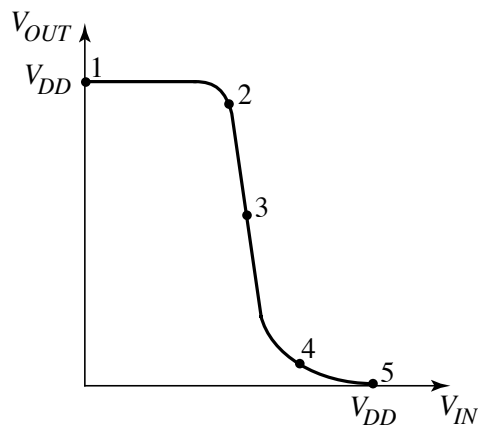
since  $i_{SUP} = -I_{Dp}$  and  $V_{SG} = V_{DD} - V_{IN}$  and  $v_{SUP} = V_{SD}$ .



# CMOS Transfer Characteristic

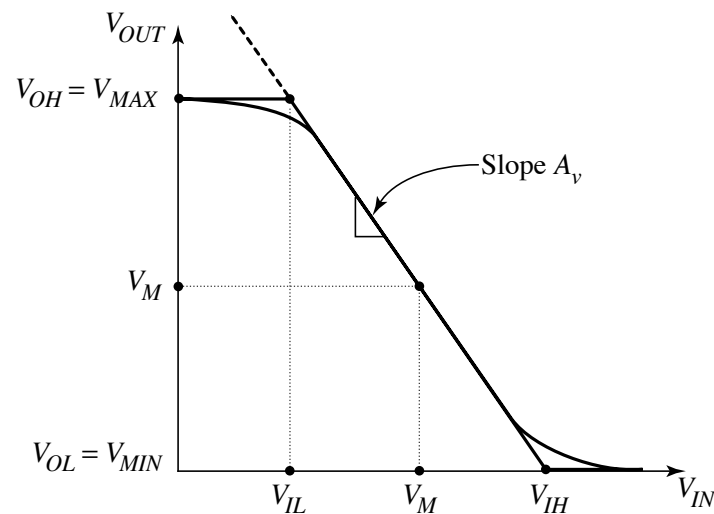
- plotting the p-channel pull-up on the n-channel “driver’s” drain characteristics allows us to find the input-output voltage pairs that satisfy the constraint that

$$I_{Dn} = -I_{Dp}$$



## Simplified Voltage Transfer Curve

- For CMOS inverters, the voltage transfer curve of the inverter is ideal enough that we can approximate it with a construction that is suitable for quick hand calculation



- We first observe that:

$$V_{OH} \approx V_{MAX} = V_{DD} \quad \text{and} \quad V_{OL} \approx V_{MIN} = 0 \text{ V}$$

The edges of the transition region are then found as the intersections of the tangent to the voltage transfer curve at  $V_{IN} = V_M$  (a line of slope  $A_v$ )

- In order to construct the VTC for a CMOS inverter (and to find estimates of the noise margins), we need to first:
  - (i) find the voltage  $V_M$
  - (ii) find the small-signal voltage gain  $A_v$  at  $V_{IN} = V_M$