

## Step 1. Finding $V_M$

- Goal: find  $V_M =$  input voltage for the output  $= V_M$

both transistors are saturated at  $V_{IN} = V_M$  since

$$V_{DSn} = V_M - 0 > V_M - V_{Tn}$$

$$V_{SDp} = V_{DD} - V_M = (V_{DD} - V_M) + V_{Tp}$$

- Equate drain currents, omitting the channel length modulation terms  $(1 + \lambda_n V_{DSn})$  and  $(1 + \lambda_p V_{SDp})$  since they tend to cancel out (if  $\lambda_n = \lambda_p$ , they exactly cancel out)

$$I_{Dn} = \mu_n C_{ox} \left( \frac{W}{2L} \right)_n (V_M - V_{Tn})^2$$

$$-I_{Dp} = \mu_p C_{ox} \left( \frac{W}{2L} \right)_p (V_{DD} - V_M + V_{Tp})^2$$

- Letting  $k_n = \mu_n C_{ox} (W/L)_n$  and  $k_p = \mu_p C_{ox} (W/L)_p$  --

$$\frac{1}{2} k_n (V_M - V_{Tn})^2 = \frac{1}{2} k_p (V_{DD} - V_M + V_{Tp})^2$$

## Finding $V_M$ (cont.)

Result:

$$V_M = \frac{V_{Tn} + \sqrt{\frac{k_p}{k_n}}(V_{DD} + V_{Tp})}{1 + \sqrt{\frac{k_p}{k_n}}}$$

We can set  $V_M = V_{DD} / 2$  and achieve a symmetrical transfer curve

Example: suppose  $V_{Tn} = -V_{Tp} = 1$  V and  $V_{DD} = 5$  V

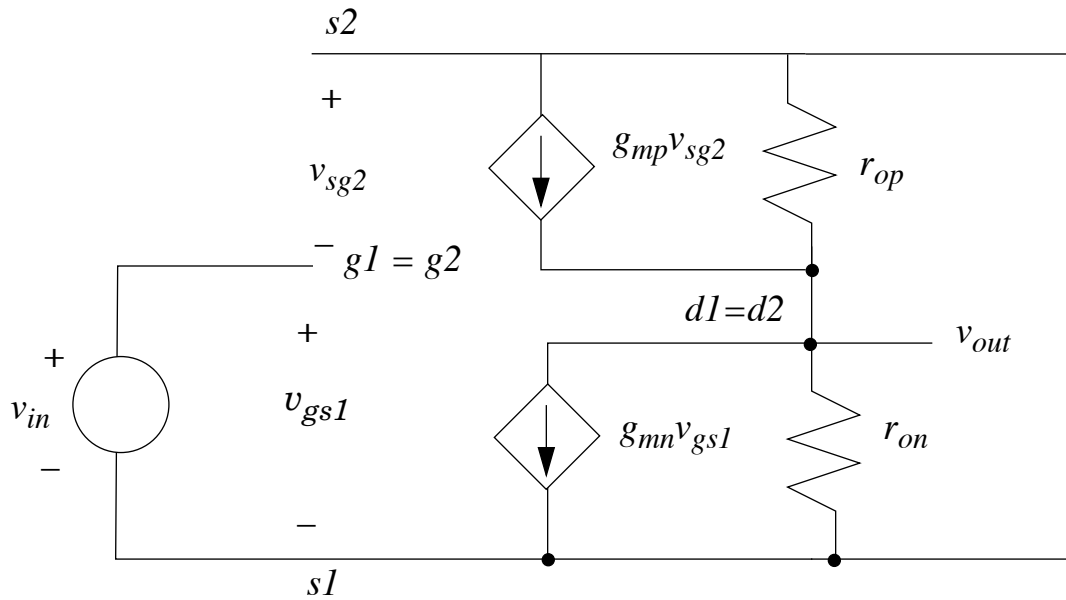
$$V_M = \frac{1 + 4 \sqrt{\frac{k_p}{k_n}}}{1 + \sqrt{\frac{k_p}{k_n}}} = 2.5 \text{ V} \rightarrow k_p = k_n$$

which makes sense since the transistors must have identical characteristics for the transfer curve to be symmetrical.

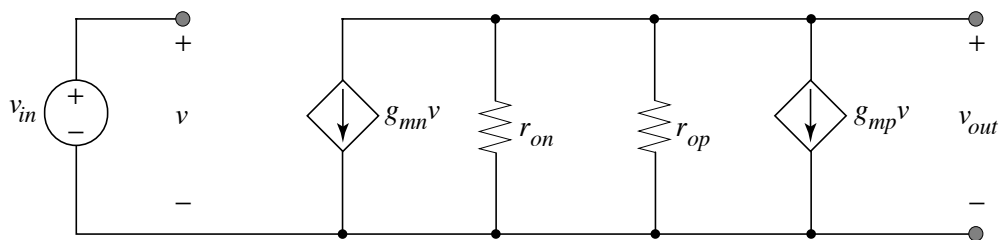
The mobility of holes in p-channels is about half that of electrons in n-channels,  $\mu_p = \mu_n / 2$ , which implies that we must adjust the width-length ratios to compensate:

$$k_n = k_p \rightarrow (W/L)_p = 2(W/L)_n$$

## Step 2. Finding $A_v$



We note that  $v_{sg2} = -v_{in}$  and can simplify the small-signal circuit



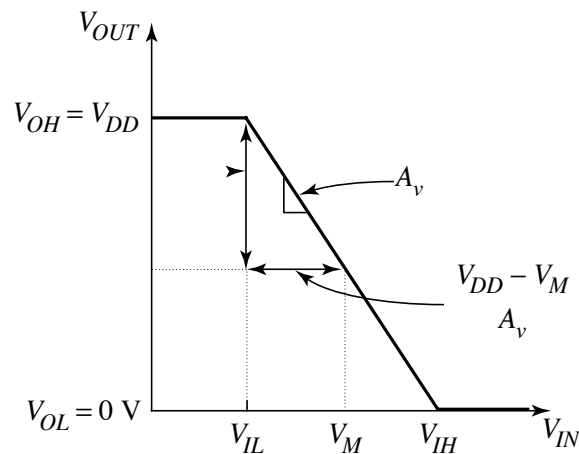
## Approximate Transfer Curve

- The small-signal gain (which is the slope of the transfer curve when the input is equal to the mid-point voltage) is:

$$v_{out}/v_{in} = -(g_{mn} + g_{mp})(r_{on} || r_{op}) = A_v$$

CMOS inverters have a channel length that is as short as possible (to minimize the area ... and maximum the density) ... the output resistances are relatively small and a typical value is  $v_{out} / v_{in} = - 5$  to  $- 10$ .

- \* The input-low and input-high voltages are:



$$V_{IL} = V_M - (V_{DD} / (2|A_v|))$$

$$V_{IH} = V_M + (V_{DD} / (2|A_v|))$$

## Noise Margins

- For  $k_N = k_P$ , the mid-point voltage is  $V_M = 2.5$  V. For a slope  $A_v = -5$ , the input-low voltage and input-high voltages are:

$$V_{IL} = 2.5 \text{ V} - (1/5) (2.5 \text{ V}) = 2 \text{ V}$$

$$V_{IH} = 2.5 \text{ V} + (1/5) (2.5 \text{ V}) = 3 \text{ V}$$

The low and high noise margins are therefore:

$$N_{ML} = V_{IL} - V_{OL} = 2 - 0 = 2 \text{ V}$$

$$N_{MH} = V_{OH} - V_{IH} = 5 - 3 = 2 \text{ V}$$

The transition region (or “gray area”) is the interval

$$V_{IL} < V_{IN} < V_{IH} \quad \text{or} \quad 2 \text{ V} < V_{IN} < 3 \text{ V}$$

- Finding the actual transfer function requires solving the drain current equations when the p-channel and n-channel are in the appropriate operating regions ... and finding the transition voltages for the regions.

SPICE is good at this job!

## CMOS Inverter: Propagation Delay

- The propagation delays  $t_{PHL}$  and  $t_{PLH}$  are obviously of major importance for digital circuit design ...

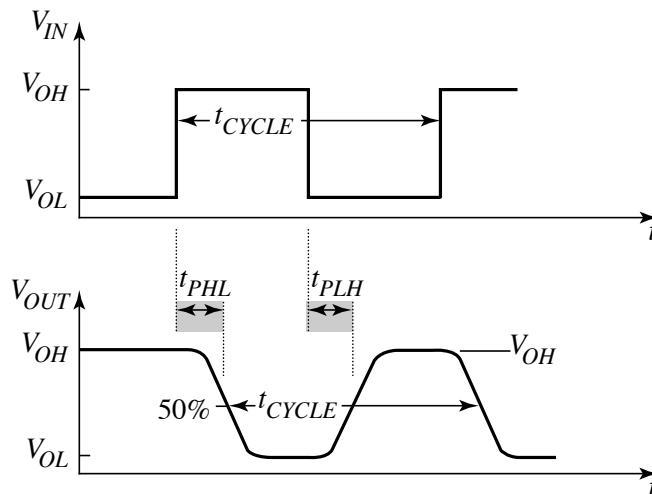
*Example:*

clock frequency = 250 MHz --> clock period = 4 ns

complex systems (e.g., microprocessor) have around 20-50 propagation delays per clock period, so we need to have

$$t_{PLH} \text{ and } t_{PHL} < 100 \text{ ps} = 10^{-10} \text{ s}$$

- Hand calculation of propagation delays: use approximation that input changes instantaneously

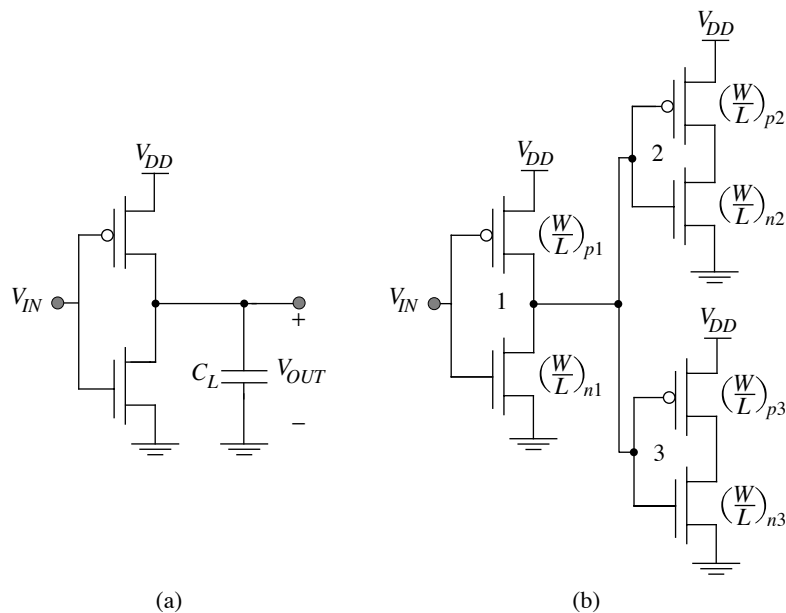


## Estimating the Load Capacitance

- The load capacitance  $C_L$  consists of

$C_G$ , the input capacitances of the inverters 2 and 3, and

$C_P$ , the parasitic capacitance to the substrate from the drain regions of inverter 1 and the interconnections between the output of inverter 1 and the inputs of inverters 2 and 3.



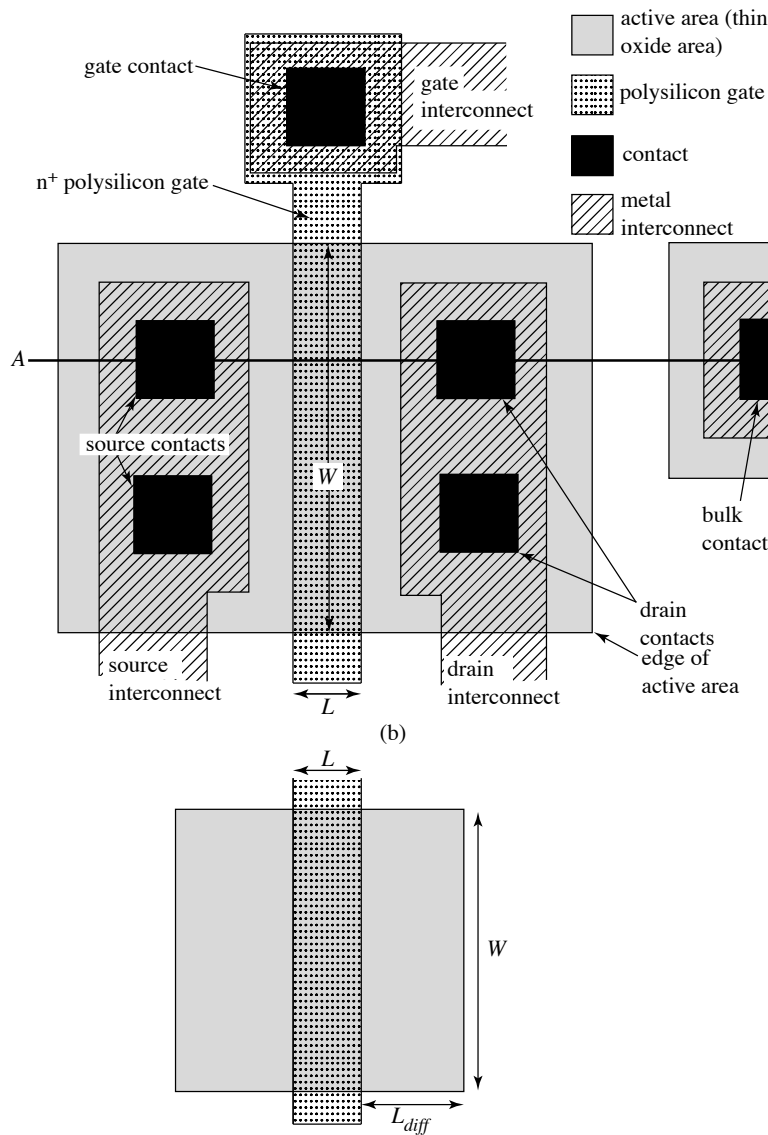
- For hand calculation, we do a worst case estimate of  $C_G$  by adding the maximum gate capacitances for inverters 2 and 3

$$C_G = C_{ox}[(W \cdot L)_{p2} + (W \cdot L)_{n2} + (W \cdot L)_{p3} + (W \cdot L)_{n3}]$$

# Parasitic Capacitance from Drain Depletion Regions

- The drain n and p regions have depletion regions whose stored charge changes during the transient.

Take the worst case and use the zero-bias depletion capacitance (the maximum value) as a linear charge-storage element during the transient.



## Calculation of Parasitic Depletion Capacitance

- “Bottom” of depletion regions of the load inverters’ drain diffusions contribute a depletion capacitance

$$C_{BOTT} = C_{Jn}(W_n L_{diffn}) + C_{Jp}(W_p L_{diffp})$$

with  $C_{Jn}$  and  $C_{Jp}$  being the zero-bias junction capacitances (fF/ $\mu\text{m}^2$ ) for the n-channel MOSFET drain-bulk junction and the p-channel MOSFET drain-bulk junction, respectively.

- “Sidewall” of depletion regions of the load inverters’ drain diffusions make an additional contribution:

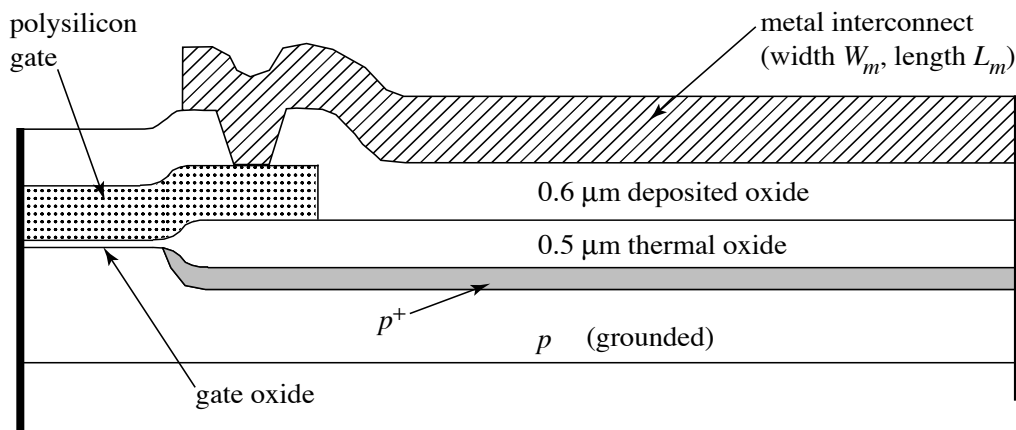
$$C_{SW} = (W_n + 2L_{diffn})C_{JSWn} + (W_p + 2L_{diffp})C_{JSWp}$$

with  $C_{JSWn}$  and  $C_{JSWp}$  being the zero-bias sidewall capacitances (fF/ $\mu\text{m}$ ) for the n-channel MOSFET drain-bulk junction and the p-channel MOSFET drain-bulk junction, respectively.

- The total depletion capacitance  $C_{DB} = C_{BOTT} + C_{SW}$
- *Typical numbers:*  $C_{Jn}$  and  $C_{Jp}$  are about 0.2 fF/ $\mu\text{m}^2$  and  $C_{JSWn}$  and  $C_{JSWp}$  are about 0.5 fF/ $\mu\text{m}$ .

## Parasitic Capacitance from Interconnections

- “Wires” consist of metal lines connecting the output of the inverter to the input of the next stage. In cross section,



- The  $p^+$  layer (i.e., heavily doped with acceptors) under the thick thermal oxide (500 nm = 0.5  $\mu\text{m}$ ) and deposited oxide (600 nm = 0.6  $\mu\text{m}$ ) depletes only slightly when positive voltages appear on the metal line, so the capacitance is approximately the oxide capacitance:

$$C_{WIRE} = C_{thickox}(W_m \cdot L_m)$$

where the oxide thickness = 500 nm + 600 nm = 1.1  $\mu\text{m}$ .

- \* For large digital systems, the parasitic interconnect capacitance can dominate the load capacitance --

$$C_L = C_G + C_P = C_G + (C_{DB} + C_{WIRE})$$