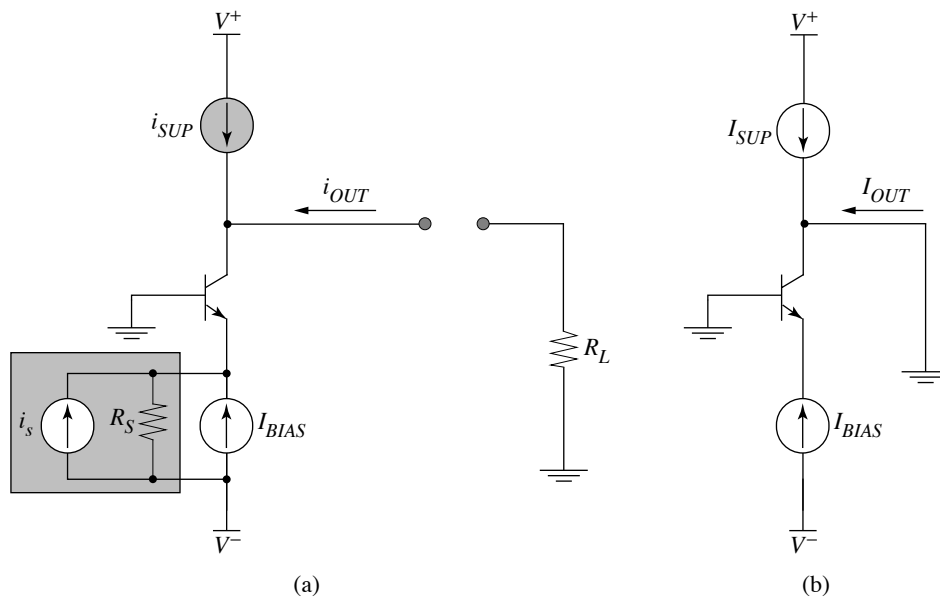


Common Base / Common Gate Amplifiers

- Input signal is applied to the emitter, output is taken from the collector
- Summary:

current gain is about unity, input resistance is low, output resistance is high

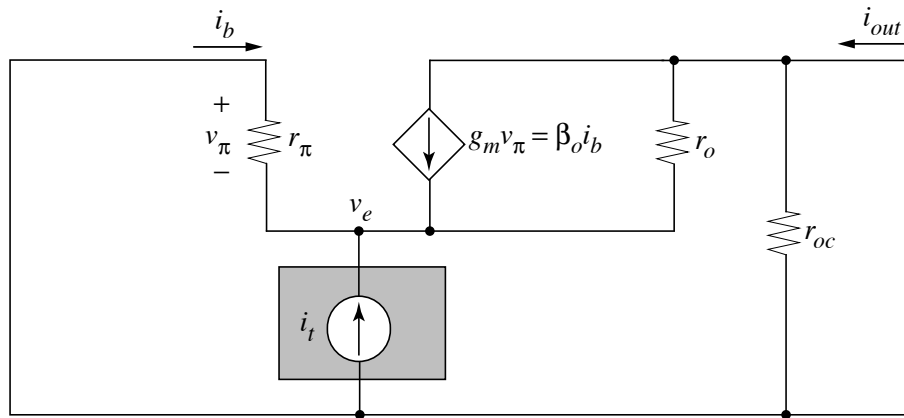
a CB stage is a good current “buffer” ... it takes a current at the input that may have a relatively small Norton resistance and replicates it at the output port, which is a good current source due to the high output resistance.



Biasing is very easy ... $I_{BIAS} = -I_{SUP}$, with a small correction factor due to the fact that β_F isn't infinity

Common-Base Current Gain A_i

- Small-signal circuit, with output shorted (according to the procedure)



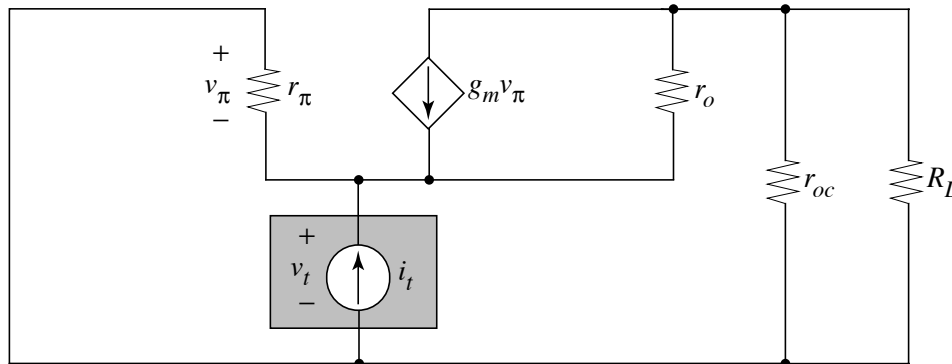
Analysis: $i_{out} = i_c \approx \beta_o i_b$ and $i_c = -i_e - i_b = -i_t - i_b = -i_t - \frac{i_{out}}{\beta_o}$

Solving for the short-circuit current gain:

$$A_i = \frac{i_{out}}{i_t} = \frac{-\beta_o}{1 + \beta_o} \cong -1$$

Common-Base Input Resistance R_{in}

- Apply test current, with load resistor R_L present at the output

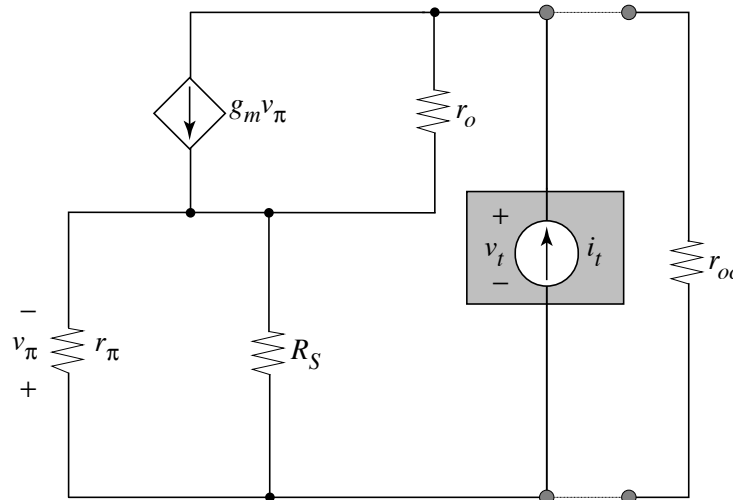


The transconductance generator dominates the sum of the currents at the input node since $g_m \gg r_o^{-1}$ and $g_m \gg r_\pi^{-1}$ and

$$R_{in} \approx \frac{1}{g_m}$$

Common-Base Output Resistance R_{out}

- Test circuit: leave source resistance of input current in place; remove r_{oc} for analysis and place it in parallel ...



- Complicated analysis (see Section 8.8), with the final result boiling down to:

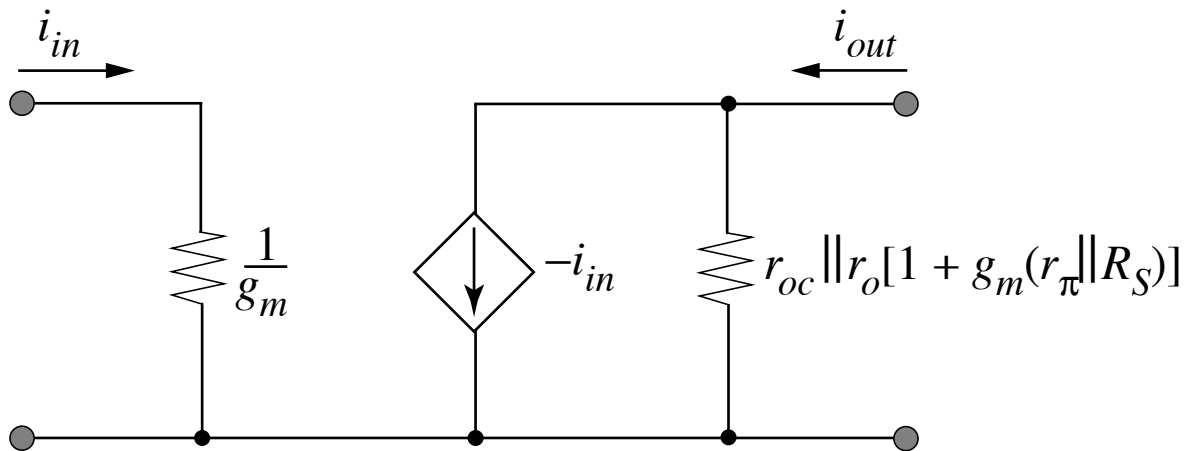
$$R_{out} \approx r_{oc} \parallel [r_o(1 + g_m(r_\pi \parallel R_S))]$$

If the R_S is much greater than r_π , then the output resistance is approximately:

$$R_{out} \approx r_{oc} \parallel [\beta r_o]$$

Common-Base Two-Port Model

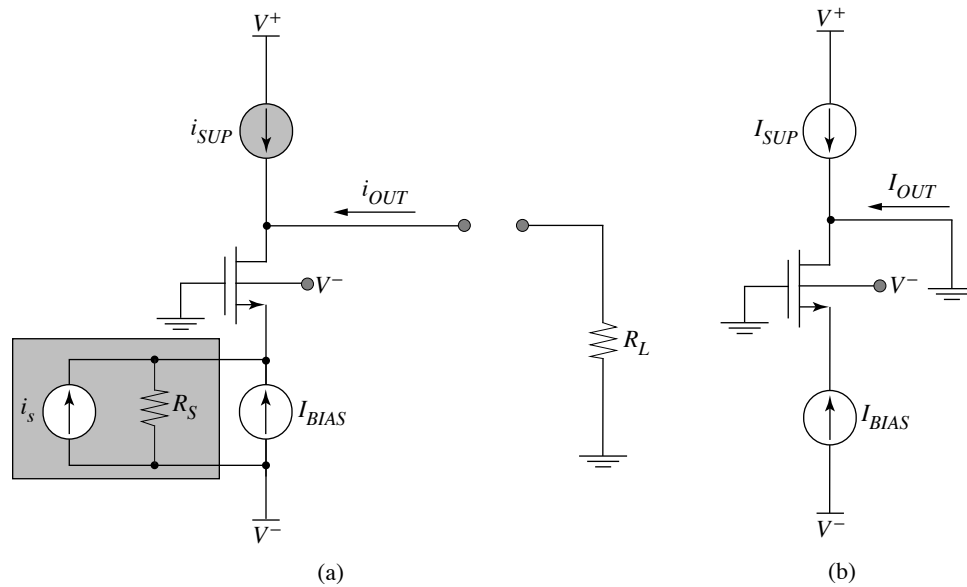
- Note that the output resistance depends on the source resistance -- which means that the CB current buffer is *not* unilateral and the two-port formal model is not strictly valid. However, the error in using the model is small (see Appendix A8.1).



- Controlled source can be flipped to make current gain + 1.

Common-Gate Amplifier

- Circuit configuration: analogous to common-base

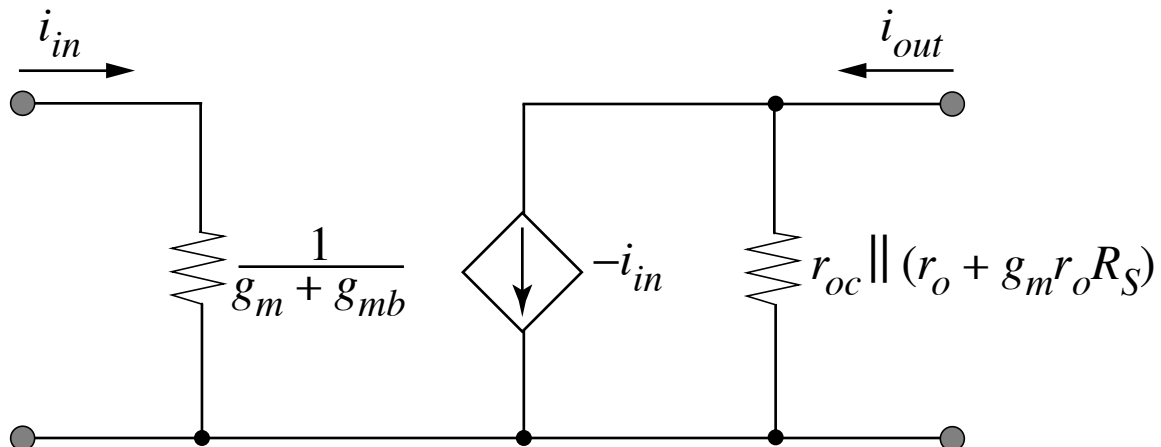


The backgate can be tied to the source if the device is in a well.

It is obvious that the current gain for this amplifier must be unity, since the gate current for a MOSFET is zero

Common-Gate Two-Port Model

- The resulting two port model is:



The input resistance is the same as for the CB for the case where source and backgate are shorted. When this isn't the case, the backgate generator is added in:

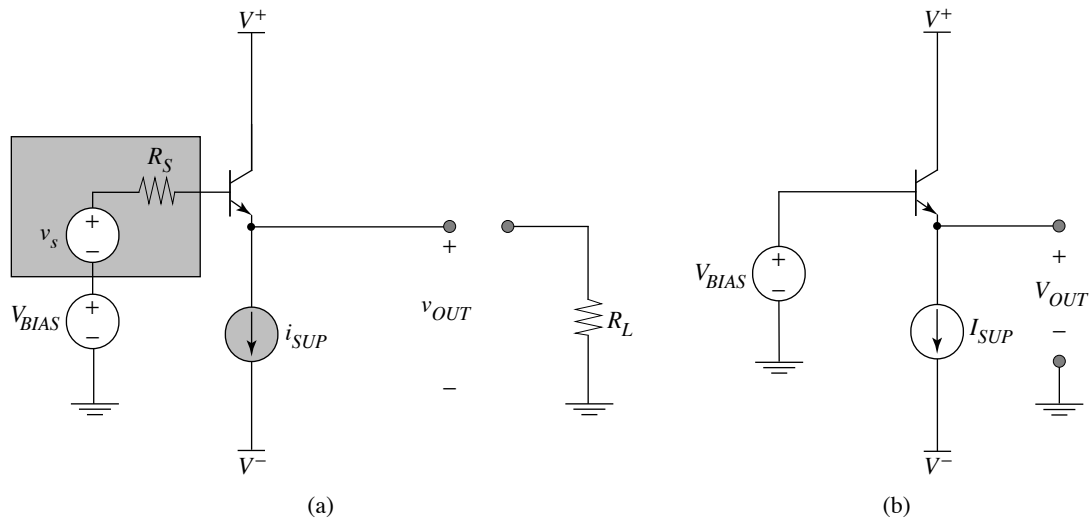
$$R_{in} = \frac{1}{g_m} \quad \text{or} \quad R_{in} = \frac{1}{g_m + g_{mb}}$$

- The output resistance is similar to the CB result with $r_{\pi} \rightarrow \infty$

$$R_{out} = r_{oc} \parallel r_o [1 + g_m R_S]$$

Common-Collector Amplifier

■ Circuit configuration

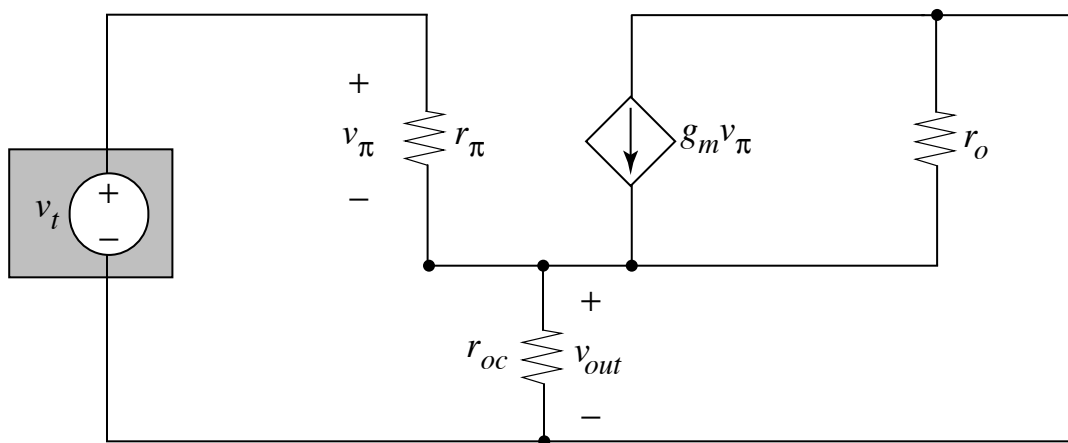


■ Biasing: if transistor is “on” (i.e., not cutoff), then

$$V_{BIAS} - V_{OUT} = 0.7 \text{ V}$$

Common-Collector as a Small-Signal Amplifier

- Linear relationship between output voltage and total input voltage indicates that the CC amplifier is a *voltage buffer* -- the voltage gain is about equal to 1.
- Small-signal model and procedure for finding A_v for two-port model:



- Circuit analysis: current through $r_{oc} \parallel r_o$ is $v_\pi / r_\pi + g_m r_\pi \rightarrow$

$$\frac{v_t - v_{out}}{r_\pi} + g_m (v_t - v_{out}) = \frac{v_{out}}{r_{oc} \parallel r_o}$$

multiplying by r_π and recognizing that $g_m r_\pi = \beta_o$,

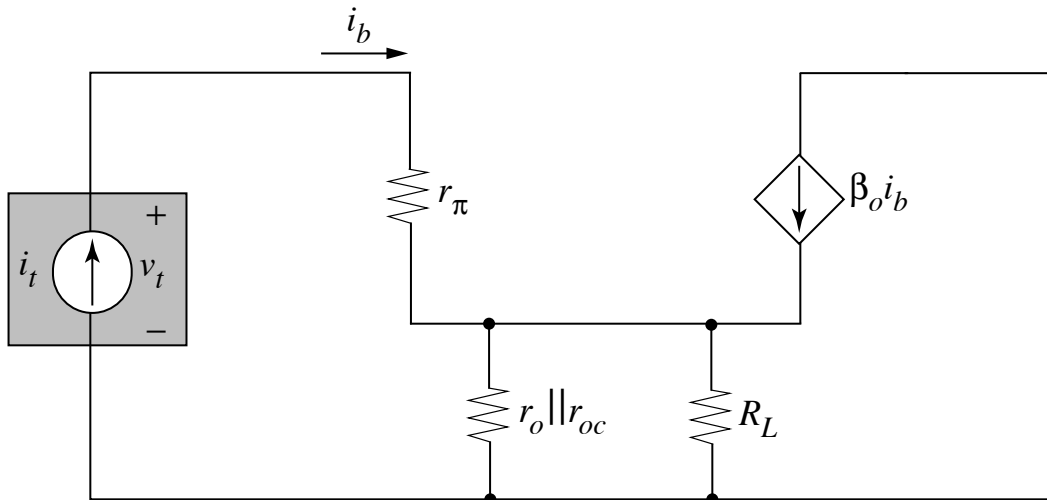
$$v_t - v_{out} + \beta_o (v_t - v_{out}) = (1 + \beta_o)(v_t - v_{out}) = \frac{v_{out} r_\pi}{r_{oc} \parallel r_o}$$

solving for the open-circuit voltage gain:

$$A_v = \frac{1}{1 + \frac{r_\pi}{r_{oc} \parallel r_o (\beta_o + 1)}} \approx 1$$

Common-Collector Input Resistance R_{in}

- Procedure: apply pure test source, leave load resistor R_L in
-- very important for CC amplifier



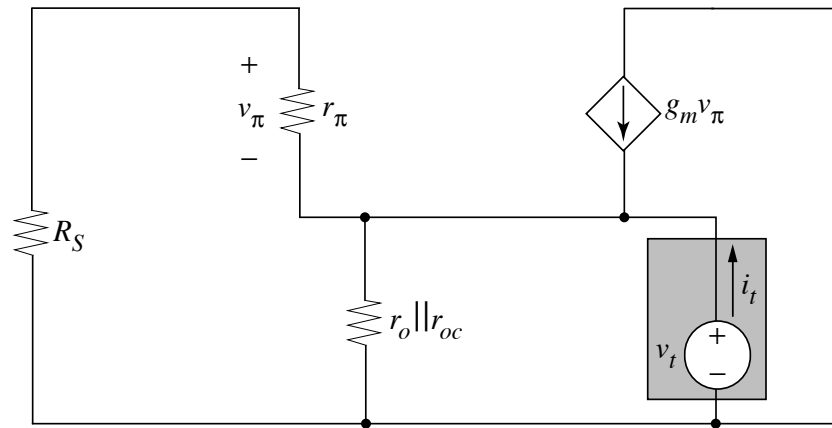
note that current through $r_{oc} \parallel r_o \parallel R_L$ is $i_t + \beta_o i_t \rightarrow$

$$R_{in} = r_\pi + (\beta_o + 1)(r_{oc} \parallel r_o \parallel R_L)$$

- When the load resistor is much smaller than the output resistance of the transistor and the current source resistance, then the input resistance of the CC amplifier is approximately $R_{in} = r_\pi + (\beta_o + 1)R_L$

Common Collector Output Resistance

- Apply test current source at the output, leaving any source resistance R_S attached at the input.

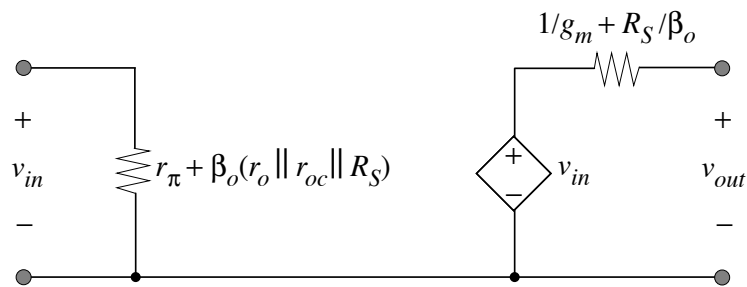


KCL at the common node + algebra -->

$$R_{out} = \frac{1}{g_m} + \frac{R_S}{\beta_o}$$

Common Collector Two-Port Model

- Final result: pretty good voltage buffer:



Note: this model is approximate and can give erroneous results for extremely low values of R_L . However, it is very convenient for hand analysis.