DC Coupling: General Trends

- **Goal**: want both input and output to be "centered" at halfway between the positive and negative supplies (or ground, for a single supply) -- in order to have maximum possible swing at the input and at the output.

  Summary of DC shifts through the single stages:

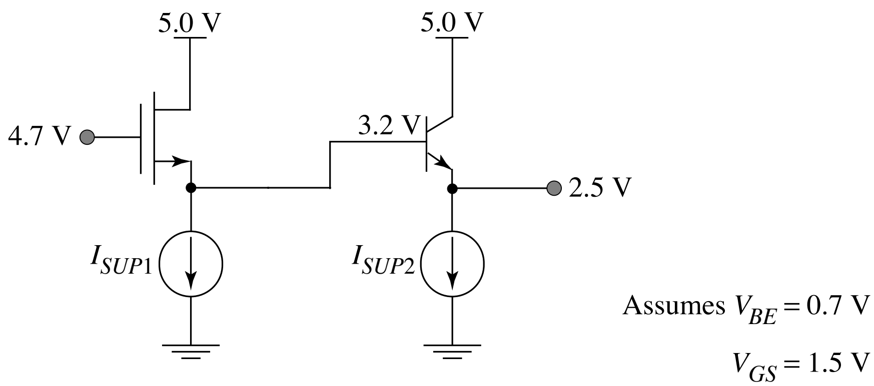
BJT Amp. Type	npn version	pnp version
CE	positive	negative
CB	positive	negative
CC	negative*	positive*

MOS Amp. Type	n-channel version	p-channel version
CS	positive	negative
CG	positive	negative
CD	negative*	positive*

The DC voltage shifts for CC/CD stages are set by the V_{BE} = 0.7 V drop or by the V_{GS} of the transistor and can be specified by the designer.

DC Coupling Example

- Common drain - common collector cascade (infinite input resistance, fairly low output resistance, unity voltage gain ... reasonable voltage buffer)



For CC stage, the optimum output voltage of 2.5 V (centered between + 5 V and ground for maximum swing) -->

$$V_{IN2} = \text{DC input of CC amp} = 2.5 + 0.7\text{ V} = 3.2\text{ V}$$

The DC of the n-channel CD amplifier is then:

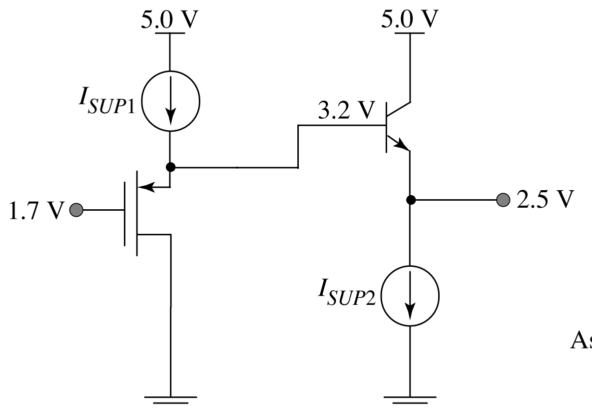
V_{IN} = DC input of CD amp = $V_{IN2} + V_{GS1}$ = 3.2 V + 1.5 V = 4.7 V

where we have assumed that V_{GS1} = 1.5 V as a typical gate-source voltage (actual number comes from I_{SUP1} and (W/L)).

- too close to the supply voltage -- input DC level should be centered at near 2.5 V.

DC Biasing Example (Cont.)

- Solution: use p-channel CD amplifier since it shifts the DC level in the **positive** direction from input to output



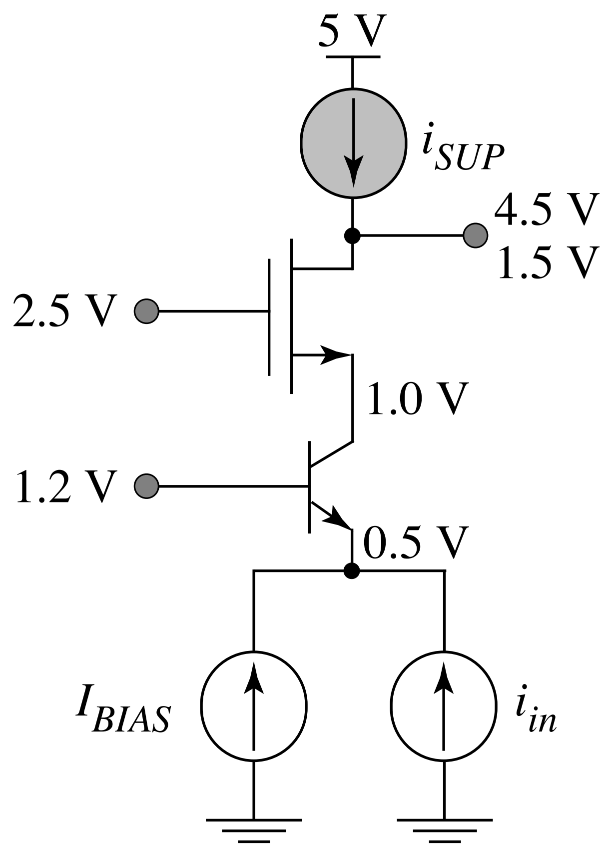
Assumes $V_{BE} = 0.7$ V

$V_{GS} = 1.5$ V

Selection of large (W/L) for the p-channel --> input DC level can be adjusted closer to 2.5 V.

Sharing a Current Supply: Current Buffer

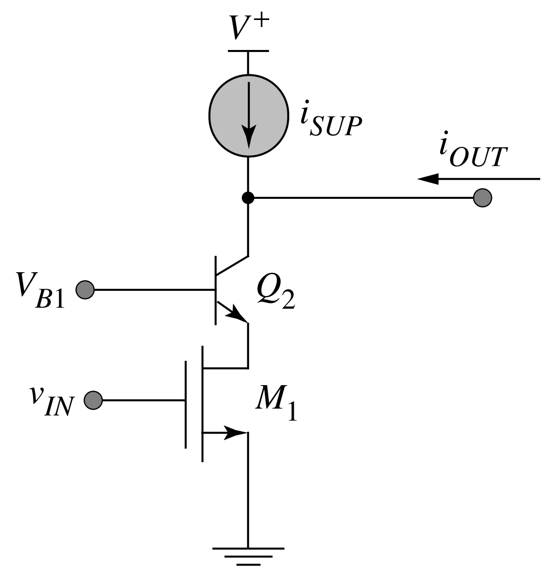
- Example: CB/CG cascade that shares common supply and bias sources



Sharing a Current Supply: the Cascode

- Common-source/common-base two-stage amplifier:

  common-source transistor is used to provide bias current to the common-base transistor



- Similar configurations are also referred to as a “cascode topology:

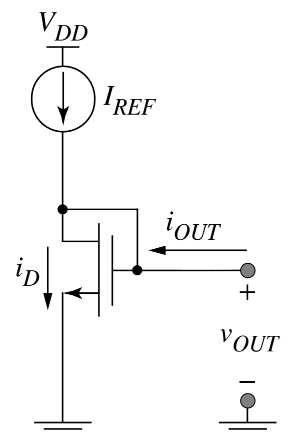
  CE/CB, CE/CG, CS/CB, and CS/CG are also cascodes

DC Voltage and Current Sources

- Output characteristic of a BJT or MOSFET look like a family of current sources ... how do we pick one?

  specify the gate-source *voltage* V_{GS} in order to select the desired current level for a MOSFET (specifiy V_{BE} for a BJT)

  how do we generate a precise voltage? ... we use a current source to set the current in a “diode-connected” MOSFET



(wait a minute ... where do we find I_{REF}? Assume that one is available)

$$i_D = I_{REF} + i_{OUT} = \left(\frac{W}{2L}\right)\mu_n C_{ox}(v_{OUT} - V_{Tn})^2$$

(neglect channel-length modulation term)

DC Voltage Sources (cont.)

- Solving for the output voltage

$$v_{OUT} = V_{Tn} + \sqrt{\frac{I_{REF} + i_{OUT}}{\left(\frac{W}{2L}\right)\mu_n C_{ox}}}$$

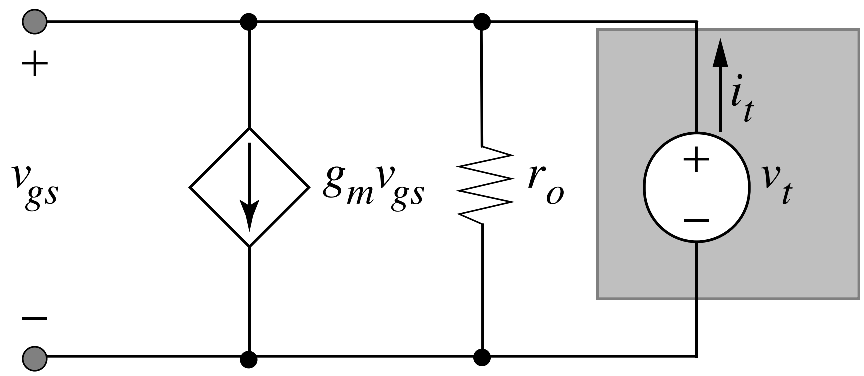
If $I_D = 100\ \mu A$, $\mu_n = 50\ \mu AV^{-2}$, $(W / L) = 20$, $V_{Tn} = 1$ V, then

$$V_{OUT} = 1.45 \text{ V for } I_{OUT} = 0 \text{ A.}$$

- bias current and MOSFET dimensions set the I_{OUT} vs. V_{OUT} characteristic

Source Resistance of Voltage Source

- Small-signal model of MOSFET with drain shorted to gate ("diode-connected")



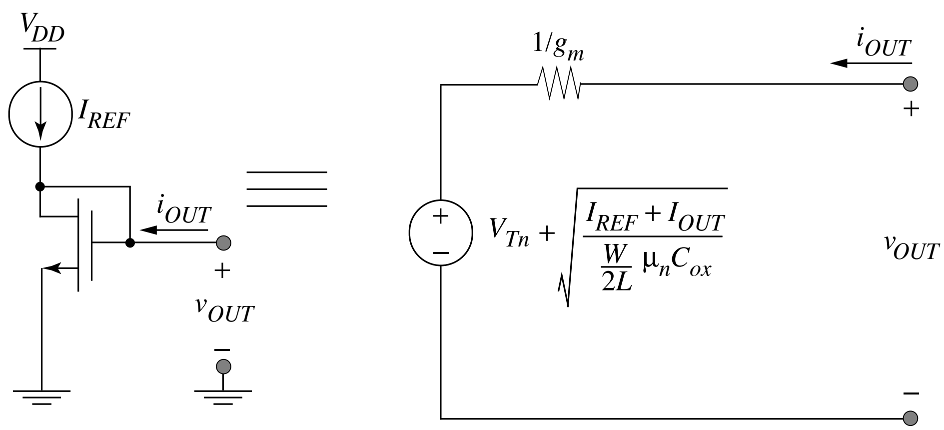
transconductance generator degenerates into a conductance
(since v_{gs} is now the voltage drop across it)

- Source resistance of voltage source (assume I_{REF} has r_{oc} --> infinity)

$$R_S = \frac{v_t}{i_t} = \frac{1}{g_m} \| r_o \approx \frac{1}{g_m}$$

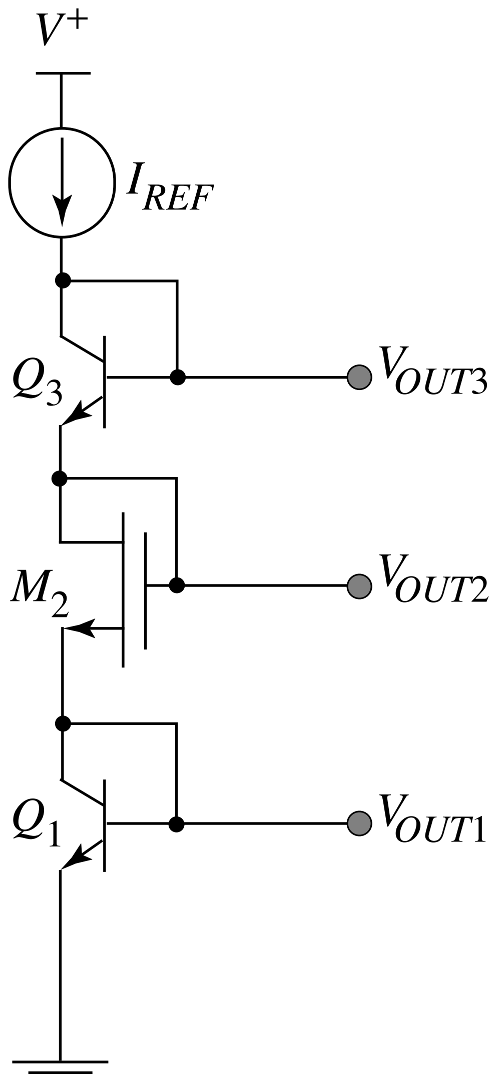
Voltage Source Equivalent Circuit (Around I_{OUT} = 0 A)

- Similar to idealized current source equivalent circuit
- Place incremental resistance $1/g_m$ in series with value of voltage source with $I_{OUT} = 0$ A



Totem Pole Voltage Sources

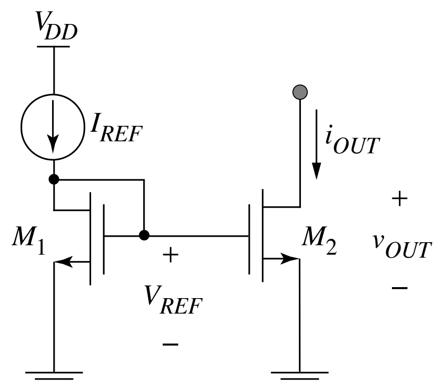
- Define a series of bias voltages between the positive and the negative supply voltages.



- In practice, output currents are small (or zero), so that the DC bias voltages are set by I_{REF}

MOSFET Current Sources

- Bias n-channel MOSFET with a DC voltage source



- Intuitively, V_{REF} is set by I_{REF} and determines the output current of M_2

$$V_{REF} = V_{Tn} + \sqrt{\frac{I_{REF}}{\left(\frac{W}{2L}\right)_1 \mu_n C_{ox}}} = V_{GS1} = V_{GS2}$$

Substituting into the drain current of M_2 (and neglecting $(1 + \lambda_n V_{DS2})$ term)

$$I_{OUT} = I_{D2} = \left(\frac{W}{2L}\right)_2 \mu_n C_{ox} (V_{GS2} - V_{Tn})^2$$

$$I_{OUT} = I_{D2} = \left(\frac{W}{2L}\right)_2 \mu_n C_{ox} \left(V_{Tn} + \sqrt{\frac{I_{REF}}{\left(\frac{W}{2L}\right)_1 \mu_n C_{ox}}} - V_{Tn} \right)^2$$

MOSFET Current Sources (cont.)

- Output current is scaled from I_{REF} by a geometrical ratio:

$$I_{OUT} = \left(\frac{(W/L)_2}{(W/L)_1}\right) I_{REF}$$