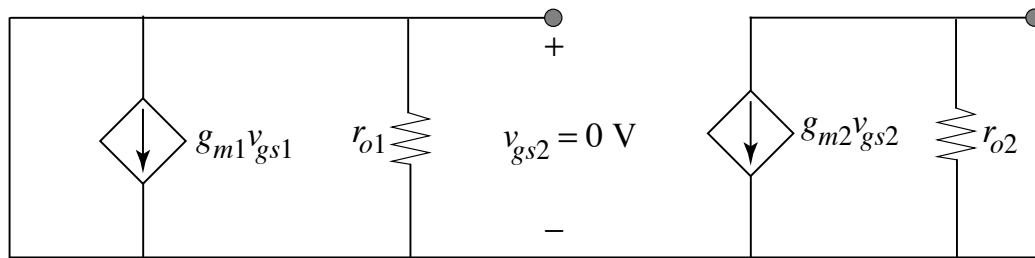
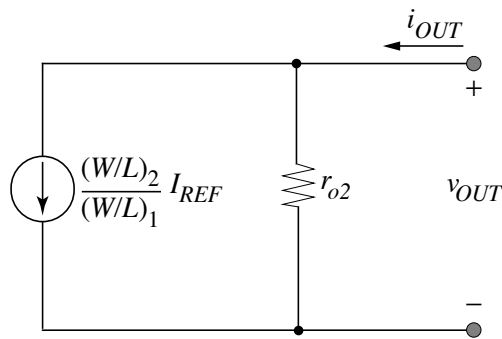


MOSFET Current Source Equivalent Circuit

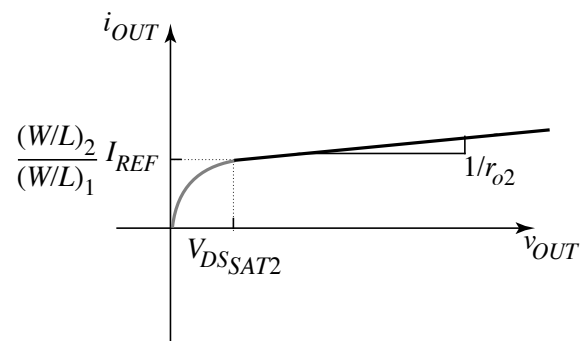
- Small-signal model: source resistance is r_{o2} by inspection



- Combine output resistance with DC output current for approximate equivalent circuit ... actual i_{OUT} vs. v_{OUT} characteristics are those of M_2 with $V_{GS2} = V_{REF}$



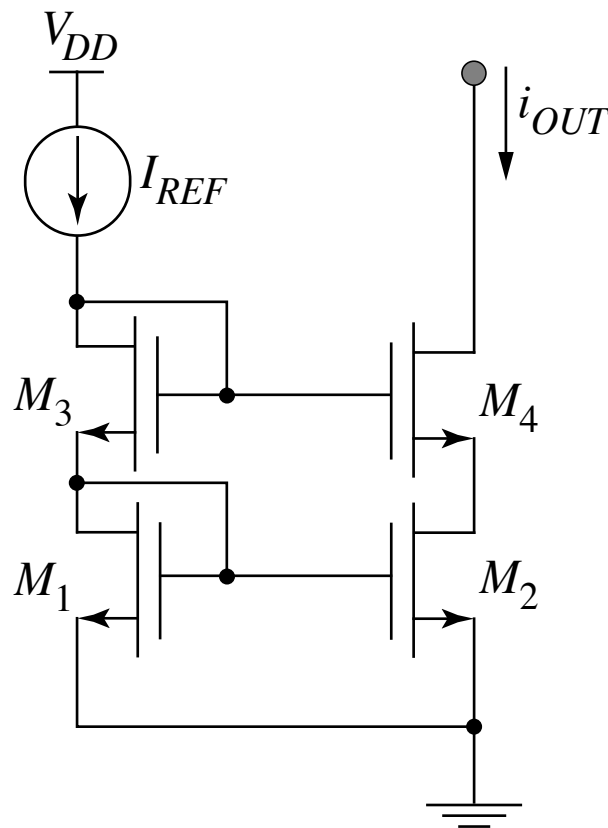
(a)



(b)

The Cascode Current Source

- In order to boost the source resistance, we can study our single-stage building blocks and recognize that a common-gate is attractive, due to its high output resistance



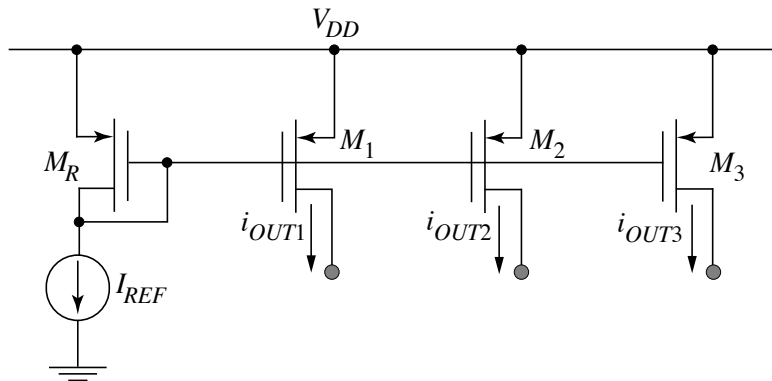
- Adapting the output resistance for a common gate amplifier, the cascode current source has a source resistance of

$$R_S = (1 + g_{m4}r_{o2})r_{o4} \approx g_{m4}r_{o4}r_{o2}$$

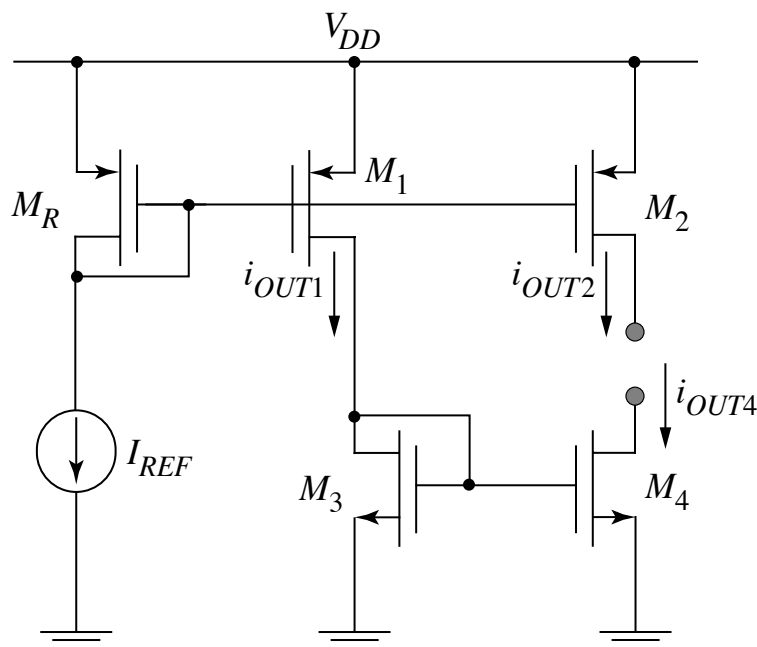
- Penalty for cascode:
needs larger V_{OUT} to function

MOSFET Current Sources and Sinks

- n-channel current source *sinks* current to ground ... how do we *source* current from the positive supply? Answer: p-channel current sources...?

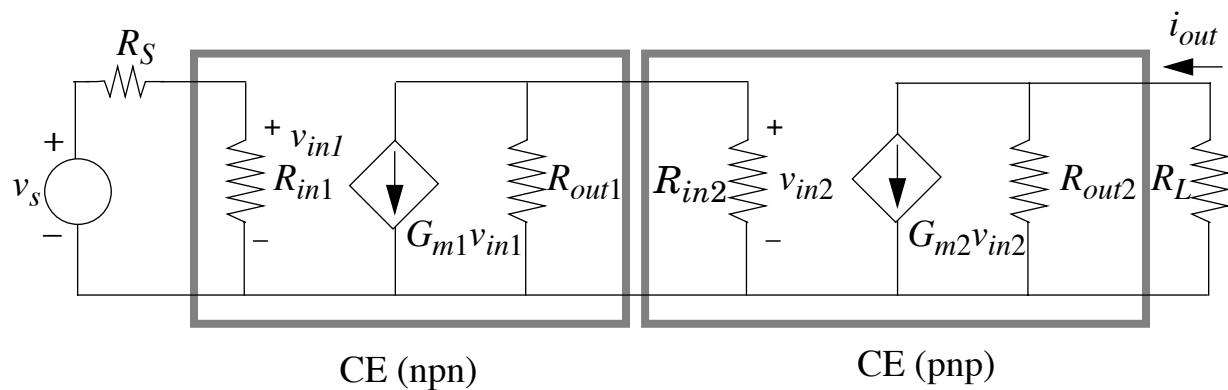


- By mixing n-channel and p-channel diode-connected devices, we can produce current sinks and sources from a reference current connected to V_{DD} or ground.



Two-Stage BiCMOS Transconductance Amplifier

- Concept: cascade two common-emitter stages to get more transconductance -- *not* an ideal solution but illustrates DC biasing and interstage coupling



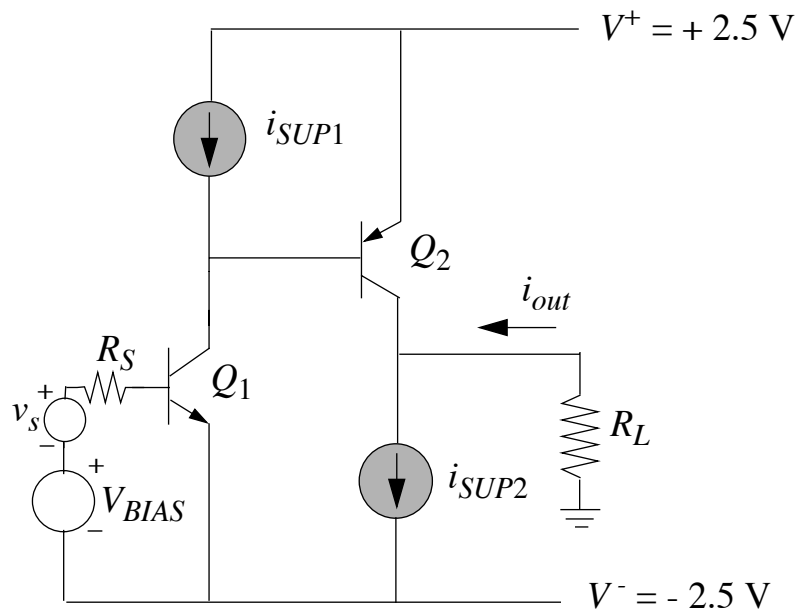
- DC Issues:

First stage: npn common-emitter amplifier (DC level shifts up)

Second stage: pnp common-emitter amplifier (DC level shifts down)

Amplifier Topology

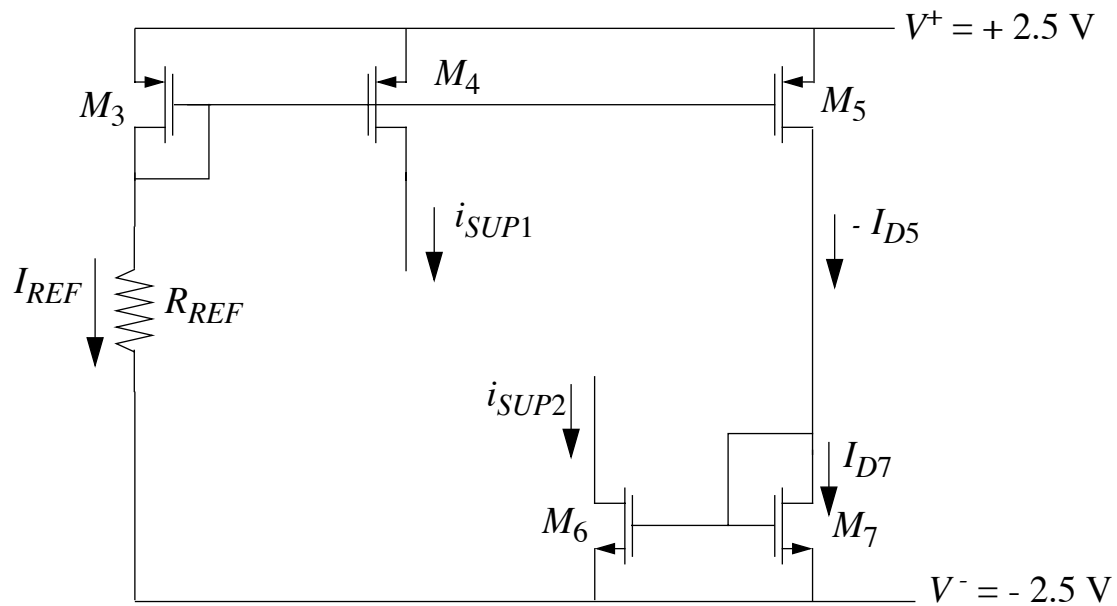
- Basic structure -- connect output of CE (npn) to input of CE (pnp), attach small-signal voltage input (with R_S) and load (R_L)



- Current source design:
assume that the reference current is generated by a resistor (to ground)

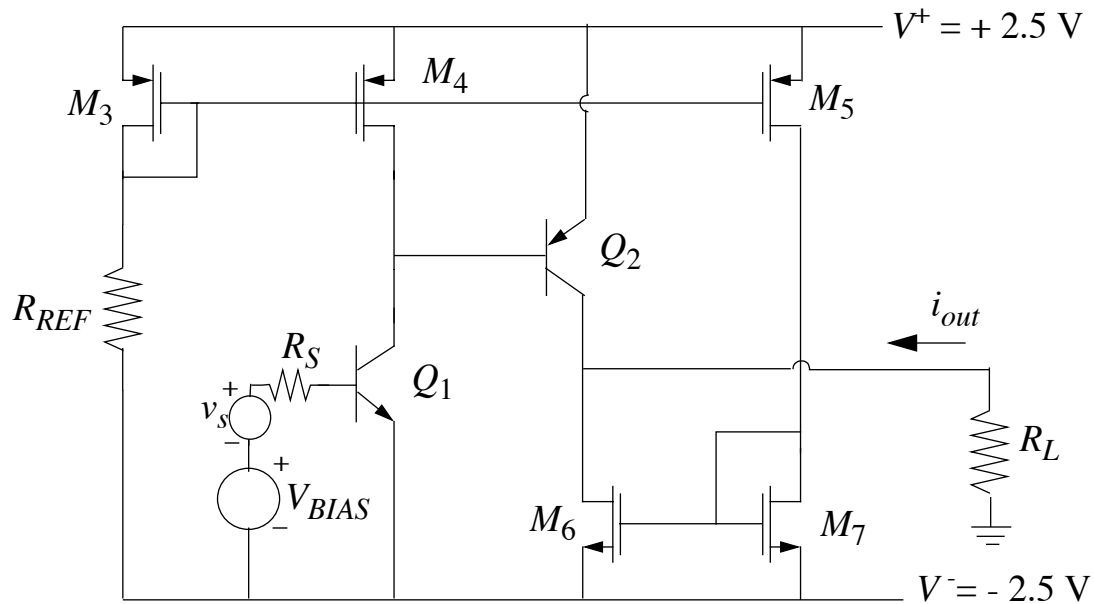
DC Currents from Reference

- p-channel diode-connected M_3 is used to generate source-gate voltages for M_4 (which generates i_{SUP1}) and for M_5 . The second current supply is generated by first using $-I_{D5}$ to generate a DC gate-source voltage via diode-connected M_7 .



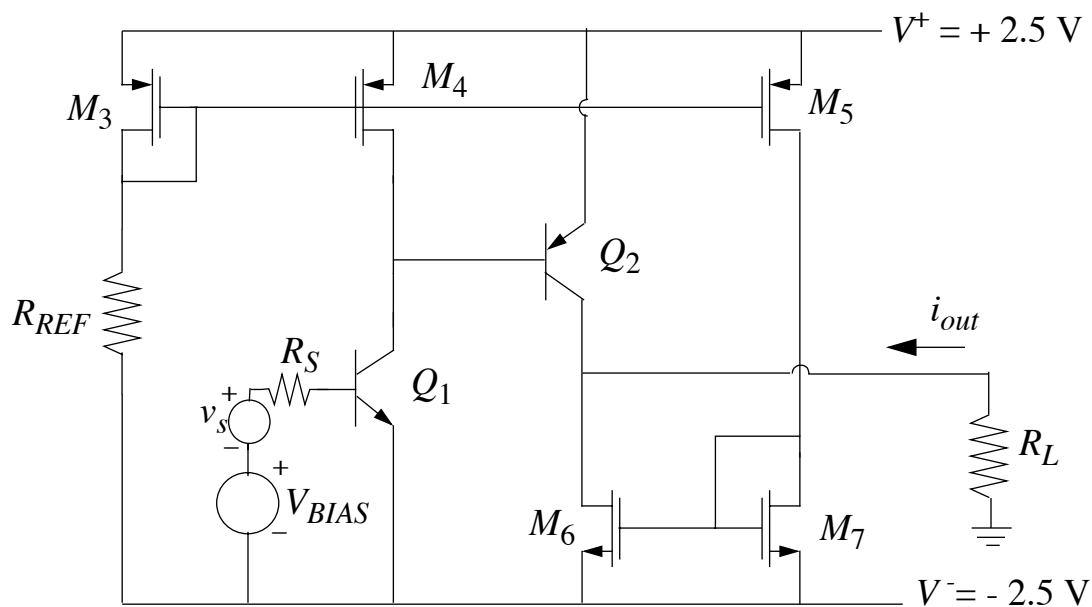
Two-Stage BiCMOS Transconductance Amplifier

- Combine current source circuit with basic amplifier topology



DC Bias of Transconductance Amplifier

- Given: $V_{OUT} = 0$ V (DC); $V^+ = 2.5$ V, $V^- = -2.5$ V; $R_S = R_L = 50$ k Ω
- Standard simplifications: assume $I_B = 0$ for bipolar transistors, neglect Early effect (BJT) and channel-length modulation (MOSFETs) for hand calculations



- Device Properties: (for simplicity, make all n-channel and all p-channel MOSFETs the same dimensions)

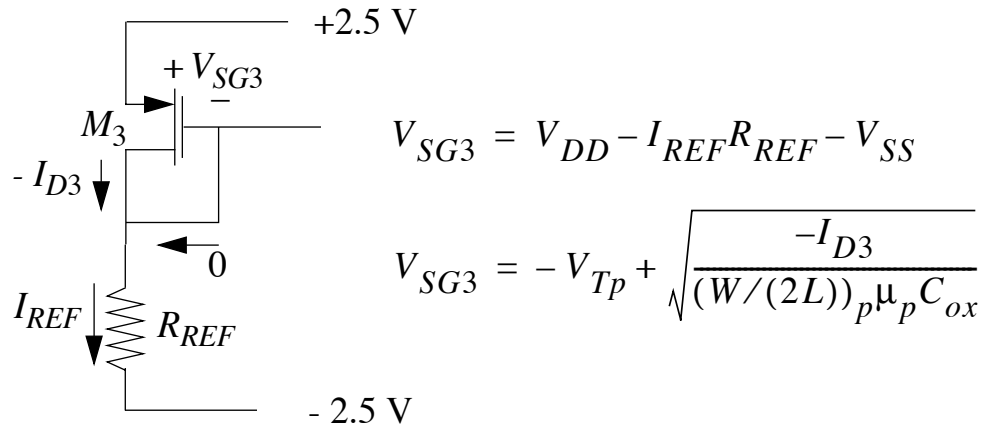
MOSFETs: $\mu_n C_{ox} = 50 \mu\text{AV}^{-2}$, $(W/L)_n = (50/2)$, $V_{Tn} = 1$ V, $\lambda_n = 0.05 \text{ V}^{-1}$

$\mu_p C_{ox} = 25 \mu\text{AV}^{-2}$, $(W/L)_p = (80/2)$, $V_{Tp} = -1$ V, $\lambda_p = 0.05 \text{ V}^{-1}$

BJTs: $\beta_{on} = 100$, $V_{An} = 50$ V, $\beta_{op} = 50$, $V_{Ap} = 25$ V

Reference Resistor

- Find R_{REF} such that $I_{REF} = 50 \mu\text{A}$ and then find all node voltages and DC bias currents ...



- Substituting $I_{REF} = -I_{D3} = 50 \mu\text{A}$, the source-gate voltage drop is

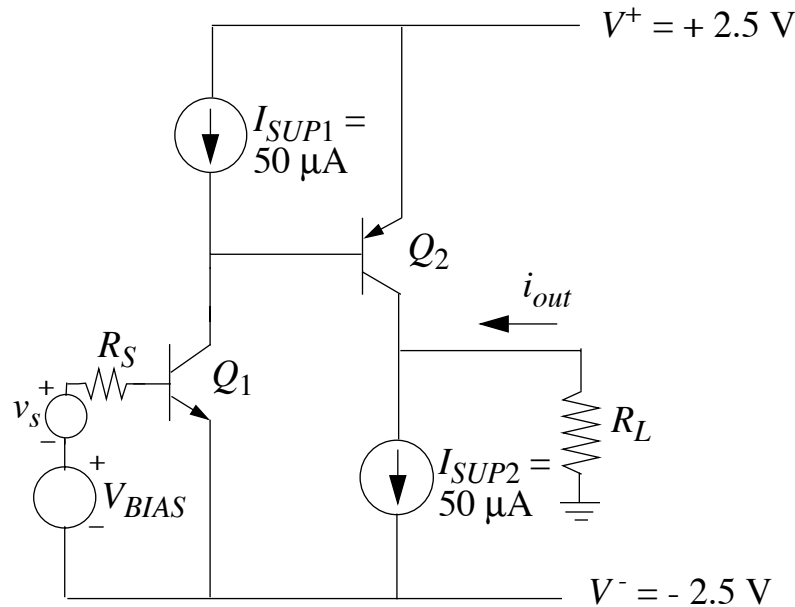
$$V_{SG3} = -(-1\text{ V}) + \sqrt{\frac{50\ \mu\text{A}}{\left(\frac{80}{(2(2))}\right)(50\ \mu\text{A}/\text{V}^2)}} = 1.22\text{ V}$$

- Solve for the reference resistor:

$$R_{REF} = \frac{(V_{DD} - V_{SS}) - V_{SG3}}{I_{REF}} = \frac{2.5\text{ V} - (-2.5\text{ V}) - 1.22\text{ V}}{50\ \mu\text{A}} = 75.6\text{ k}\Omega$$

DC Operating Point

- Since width-to-length ratios are identical for n-channel and p-channel devices (separately), the DC supply currents are equal to the reference current



- Neglecting base currents, $I_{C1} = 50 \mu\text{A}$ and $I_{C2} = 50 \mu\text{A}$

$$Q_1: g_{m1} = 2 \text{ mS}, r_{\pi 1} = 50 \text{ k}\Omega, r_{o1} = 1 \text{ M}\Omega$$

$$Q_2: g_{m2} = 2 \text{ mS}, r_{\pi 2} = 25 \text{ k}\Omega, r_{o2} = 500 \text{ k}\Omega$$

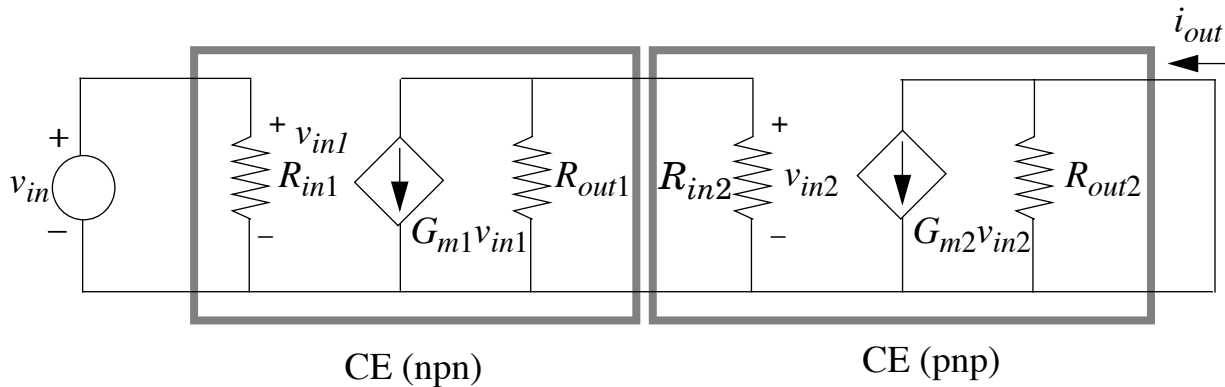
Source resistances of the current supplies for first and second stages:

$$r_{oc1} = r_{o4} = (\lambda_4(-I_{D4}))^{-1} = (0.05(0.05))^{-1} = 400 \text{ k}\Omega$$

$$r_{oc2} = r_{o6} = (\lambda_6(I_{D6}))^{-1} = (0.05(0.05))^{-1} = 400 \text{ k}\Omega$$

Overall Two-Port Model

- $R_{in} = R_{in1} = 50 \text{ k}\Omega$ and $R_{out} = R_{out2} = r_{o2} \parallel r_{oc2} = 500 \text{ k}\Omega \parallel 400 \text{ k}\Omega = 220 \text{ k}\Omega$
- Overall short-circuit transconductance G_m -- must apply procedure



Find input voltage to the second stage:

$$v_{in2} = -G_{m1}(R_{out1} \parallel R_{in2})v_{in} = -g_{m1}(r_{o1} \parallel r_{oc1} \parallel r_{\pi 2})v_{in}$$

Output current

$$i_{out} = G_{m2}v_{in2} = g_{m2}[-g_{m1}(r_{o1} \parallel r_{oc1} \parallel r_{\pi 2})]v_{in}$$

- Overall transconductance:

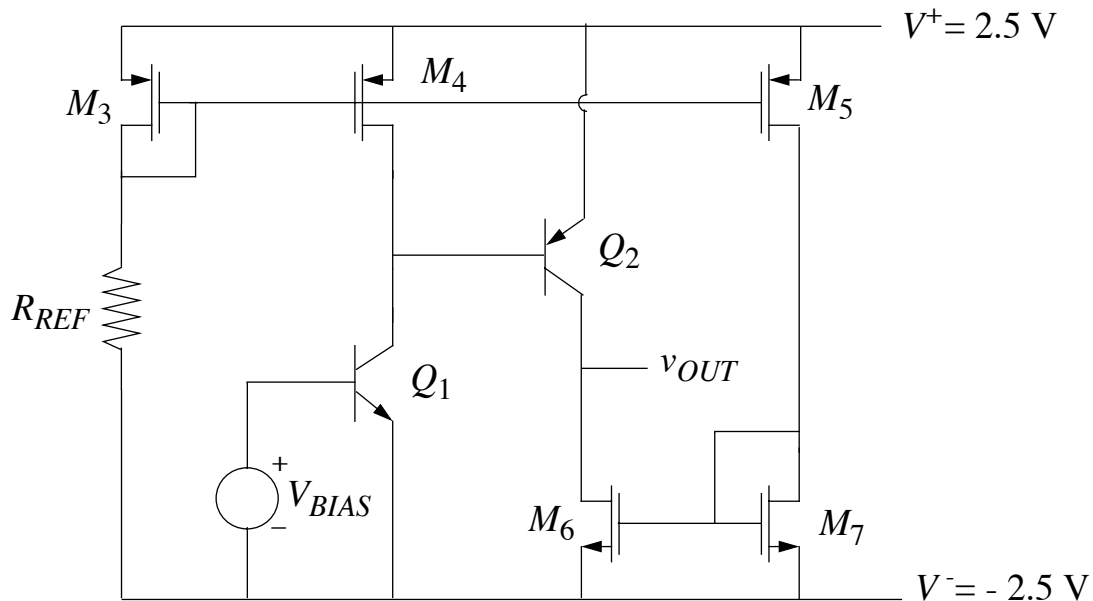
$$G_m = i_{out} / v_{in} = -g_{m2}g_{m1}(r_{o1} \parallel r_{oc1} \parallel r_{\pi 2})$$

$$G_m = -(2 \text{ mS})(2 \text{ mS})(1 \text{ M}\Omega \parallel 400 \text{ k}\Omega \parallel 25 \text{ k}\Omega) = -(2 \text{ mS})(2 \text{ mS})(23 \text{ k}\Omega)$$

$$G_m = -92 \text{ mS}$$

Output Voltage Swing

- Find the maximum and minimum values of v_{OUT}



- Determine how high the output node can rise before a device leaves its constant-current region

$$Q_2 \text{ saturates when } v_{OUT} = V_{OUT(max)} = 2.4\text{ V} \dots V_{EC(sat)} = 0.1\text{ V}$$

$$\text{Note that } M_4 \text{ is still saturated since } V_{SD4} = V_{EB4} = 0.7\text{ V} > v_{SG4} + V_{Tp} = 0.22\text{ V}$$

- Determine how low the output node can drop ...

$$M_6 \text{ goes triode when } v_{OUT} = V_{DS7(sat)} = V_{GS7} - V_{Tn} = 1.22\text{ V} - 1\text{ V} = 0.22\text{ V}$$

$$V_{OUT(min)} = -2.5\text{ V} + 0.22\text{ V} = -2.28\text{ V}$$