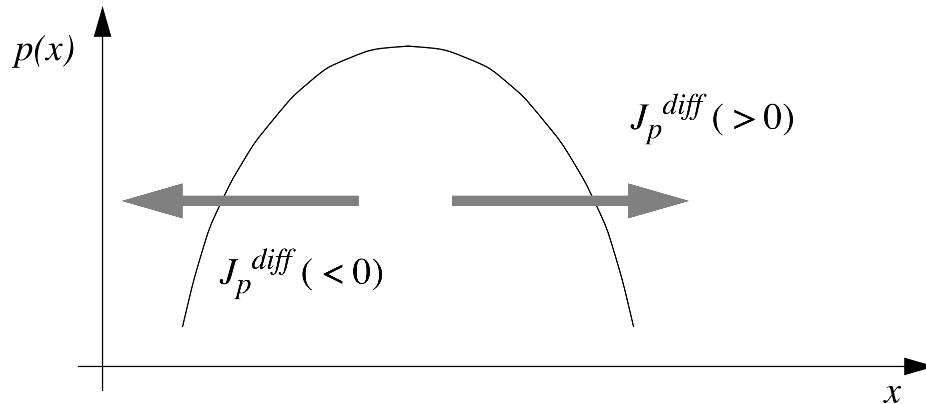
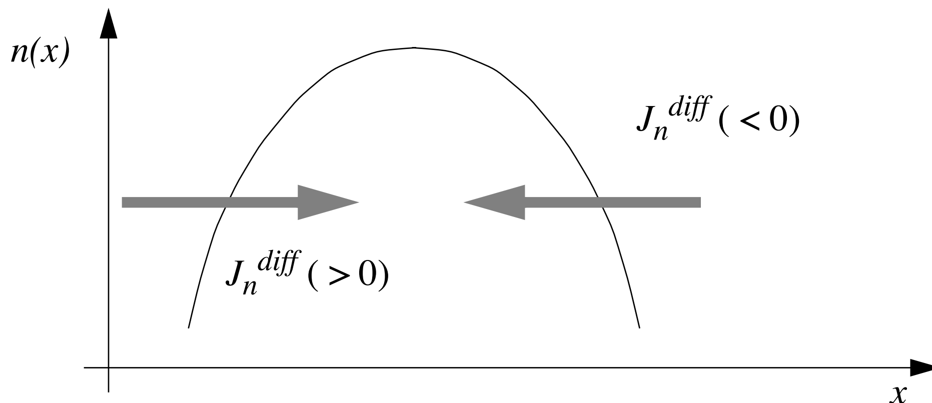
Carrier Transport by Diffusion

- Holes diffuse "down" the concentration gradient and carry a positive charge --> hole diffusion current has the *opposite* sign to the gradient in hole concentration dp/dx



- Electrons diffuse down the concentration gradient, yet carry a negative charge --> electron diffusion current density has the *same* sign as the gradient in electron concentration dn/dx.



Electron Diffusion Current Density

- Similar analysis leads to

$$J_n^{diff} = qD_n \frac{dn}{dx},$$

where D_n is the electron diffusion coefficient (units: cm^2/s)

- Numerical values of diffusion coefficients: use Einstein's relation

$$\boxed{\frac{D_n}{\mu_n} = \frac{kT}{q}}$$

- The quantity kT/q has units of volts and is called the *thermal voltage*, V_{th}:

$$V_{th} = \frac{kT}{q} = 25 - 26\,\text{mV},$$

at "room temperature," with 25 mV for a cool room (62 ^{o}F) and 26 mV for a warm room (83 ^{o}F).

We will pick 25 mV or 26 mV depending on which gives the "roundest" numbers.

Total Current Densities

- Add drift and diffusion components for electrons and for holes --

$$J_n = J_n^{dr} + J_n^{diff} = qn\mu_n E + qD_n \frac{dn}{dx}$$

$$J_p = J_p^{dr} + J_p^{diff} = qp\mu_p E - qD_p \frac{dp}{dx}$$

- Fortunately, we will be able to eliminate one or the other component of the electron or the hole current in our analysis of semiconductor devices.

IC Fabrication Technology

- History:

1958-59: J. Kilby, Texas Instruments and R. Noyce, Fairchild
1959-70: Explosive growth in US (bipolar ICs)
1970-85: MOS ICs introduced, RAMs, microprocessors, Japan catches up to US in volume
1985-95: PC revolution, improved design software for complex CMOS integrated systems, US leads in microprocessors, Japan in RAMs
1996-2000 > 10^8 devices/chip (= 1000 Mbit dRAM), US remains competitive -- even dominates -- sectors of the market; spin-offs from IC technology in MEMS (micro electro-mechanical systems) for sensing acceleration

- Key Idea: *batch fabrication* of electronic circuits

An entire circuit, say 10^6 transistors and associated wiring -- can be made in and on top of a single silicon crystal by a series of process steps similar to printing.

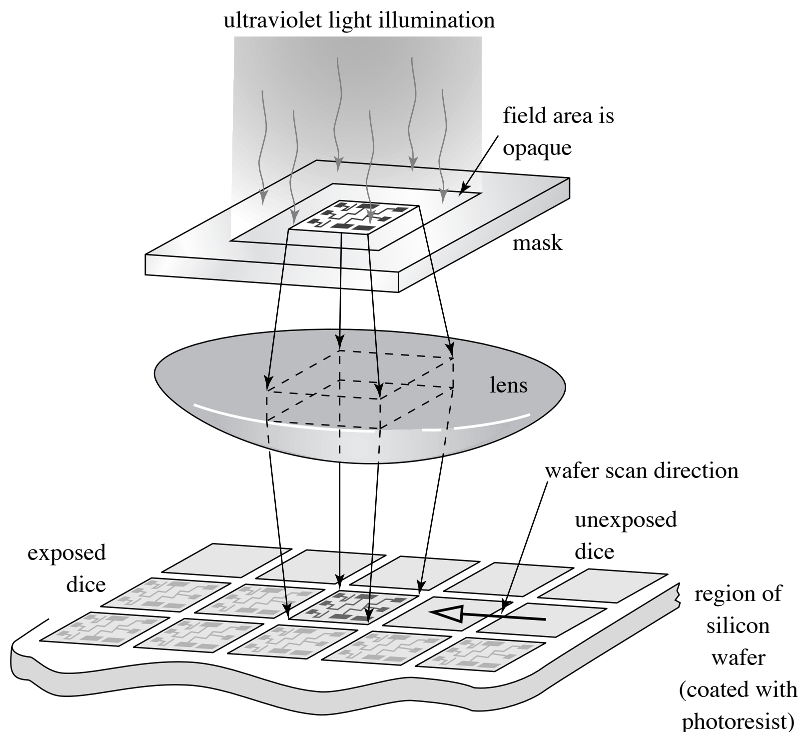
The silicon crystal is a thin disk about the size of a small dinner plate (ca. 1996) called a *wafer*. More than 100 copies of the circuit are made at the same time.

- Results:

1. Complex systems can be fabricated reliably
2. Cost per function drops as the process improves (e.g., finer printing), since the cost per processed wafer remains about the same

Photolithography

- The essential process step: makes possible the transfer of a series of patterns onto the wafer -- all aligned to within 0.1 μm
- Process "Tool" -- *wafer stepper*



- UV-sensitive film is called *photoresist*. Regions exposed to UV dissolve in developer (for *positive* photoresist -- the type we will consider)

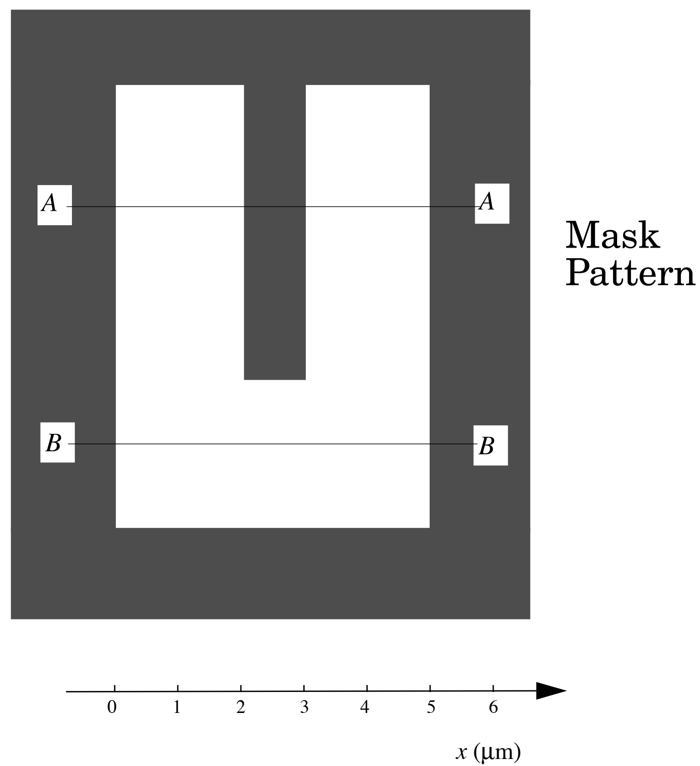
Exposure, Development, and Pattern Transfer

- Simple example of a *layout* and a *process* (or *recipe*)

  * *Layout* is the set of mask patterns for particular layers (one in this case)

  * *Process* is the sequence of fabrication steps

- Visualize by generating *cross sections* through the structure as it is built up through the process



Process Flow in Cross Sections

- Process (simplified)

  0. Clean wafer in nasty acids (HF, HNO_3, H_2SO_4, ...) --> wear gloves!

  1. Grow 500 nm of SiO_2 (by putting the wafer in a furnace with O_2

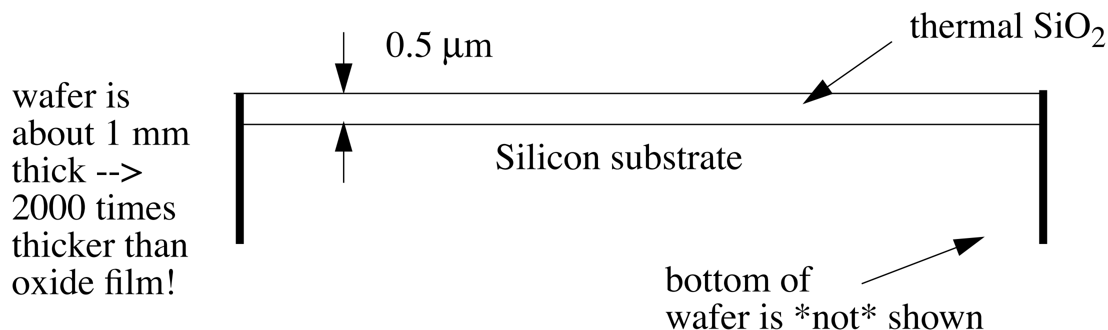
  2. Coat the wafer with 1 μm of photoresist

  3. Expose and develop the image and bake the resist to get rid solvent and to make it tougher

  4. Put wafer in a plasma etcher -- fluorine ions in plasma etch SiO_2 much faster than underlying silicon -- and etch off exposed SiO_2

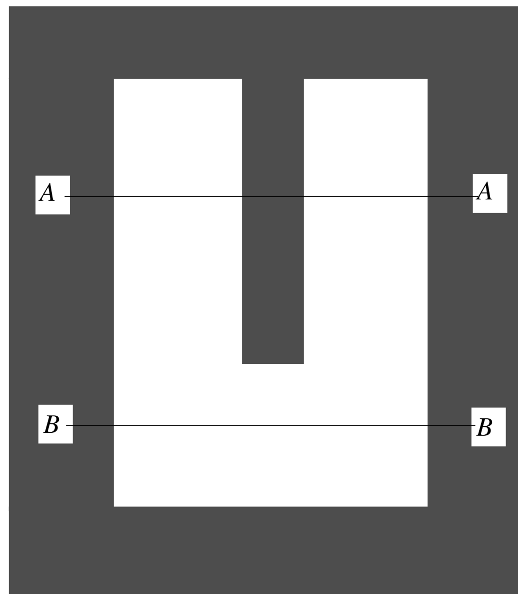
  5. Put wafer in a plasma stripper -- oxygen ions remove photoresist and leave SiO_2 untouched.

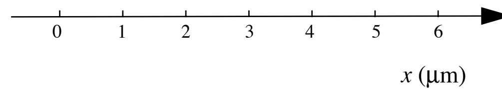
- After Step 1 (SiO_2 growth):

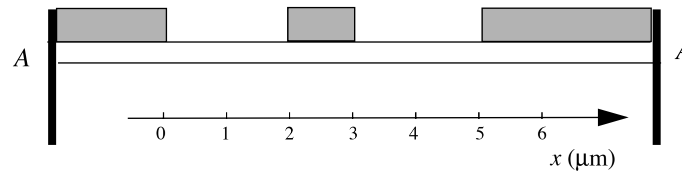


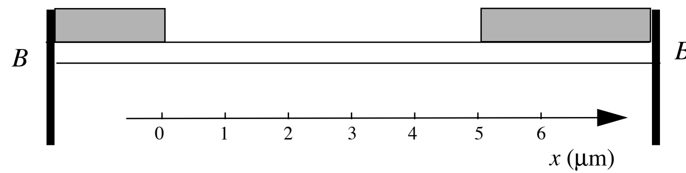
Process Flow (cont.)

- After Step 3: photoresist has been developed from clear areas of the mask



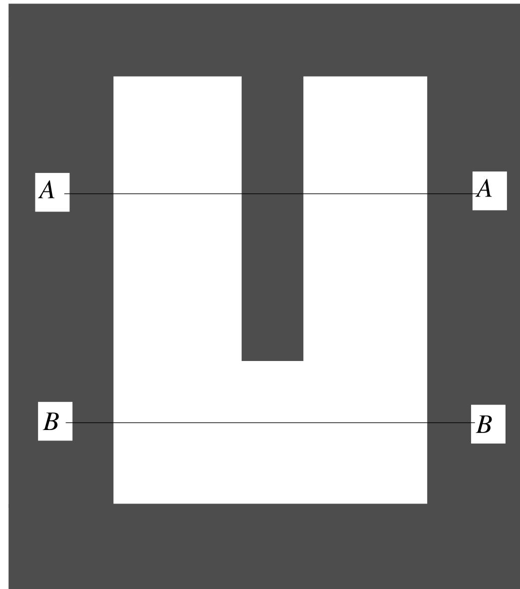


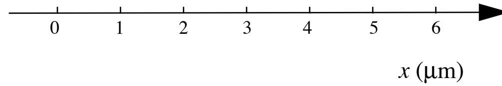


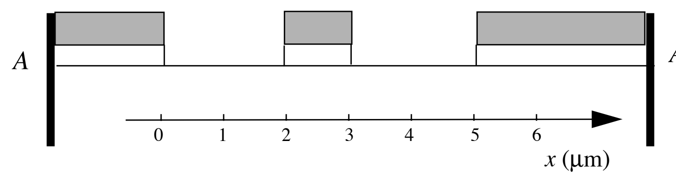


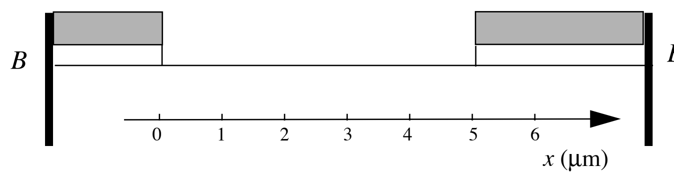
Process Flow (cont.)

- After Step 4: oxide is etched in the fluorine plasma, without etching of the underlying silicon









Completed Structure

- After Step 5: oxygen plasma strips (i.e., etches) the photoresist