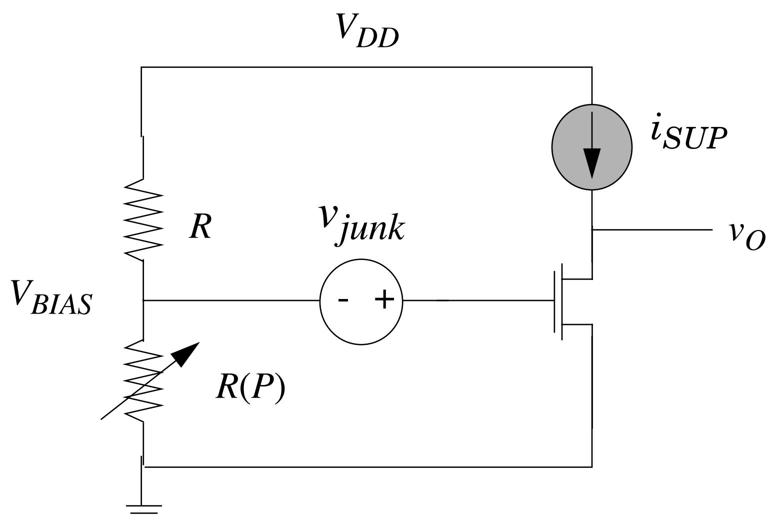
Why Use Differential Amplifiers?

- Single-ended detection using a variable resistor

  1. need to consider DC level ... sets V_{BIAS}

  2. “junk” pickup (antenna) on possibly *long* interconnection -->
     appears at the amplifier input



$R(P)$ represents a pressure-sensitive resistor

$$R(P) = R + \Delta R \text{ where } \Delta R \propto P$$

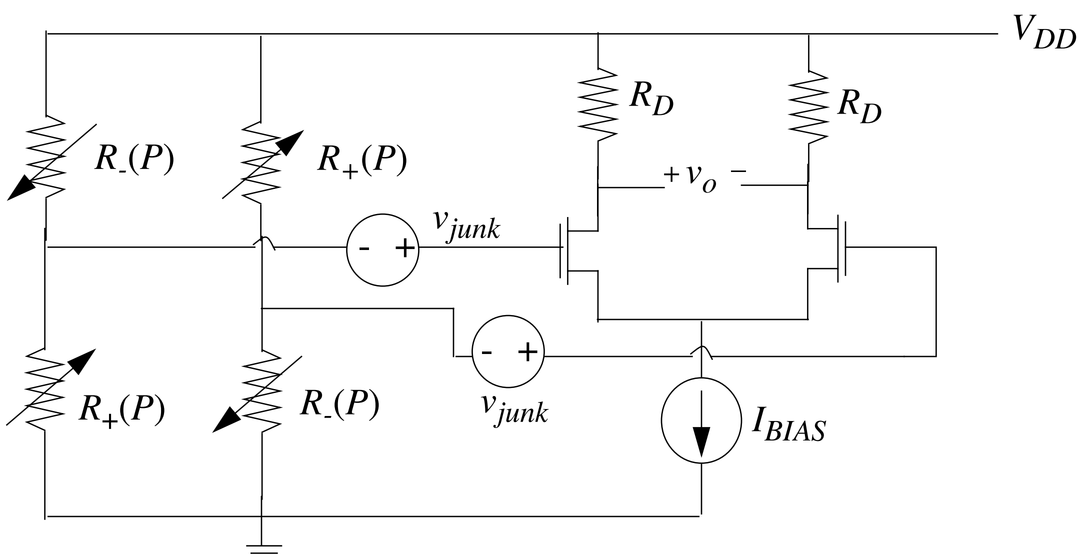
another example: a temperature-sensitive resistor = “thermistor”

Differential Interface Circuit

- Use Wheatstone bridge: voltage on one side goes up with pressure; voltage on the other side goes down

$$R_+(P) = R + \Delta R \text{ and } R_-(P) = R + \Delta R$$

- Use a differential amplifier as the input stage



- Interfering voltage v_{junk} is *common* to both inputs of the differential pair:

$$v_{ID} = \left\{V_{DD}\left(\frac{R + \Delta R}{R - \Delta R + R - \Delta R}\right) + v_{junk}\right\} - \left\{V_{DD}\left(\frac{R - \Delta R}{R + \Delta R + R - \Delta R}\right) + v_{junk}\right\}$$

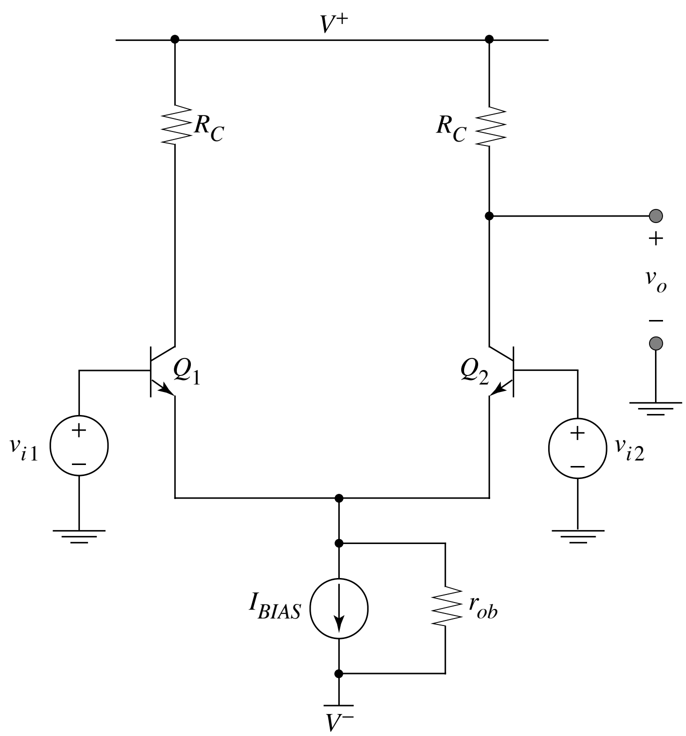
$$v_{id} = V_{DD}\left(\frac{2\Delta R}{2R}\right) = V_{DD}\left(\frac{\Delta R}{R}\right)$$

- Note that v_{junk} is common to both inputs and is rejected by the CMRR of the amplifier

Differential Amplifier with Single-Ended Outputs

- An output voltage referenced to ground is important in some applications

  Simple approach: take the output from one side



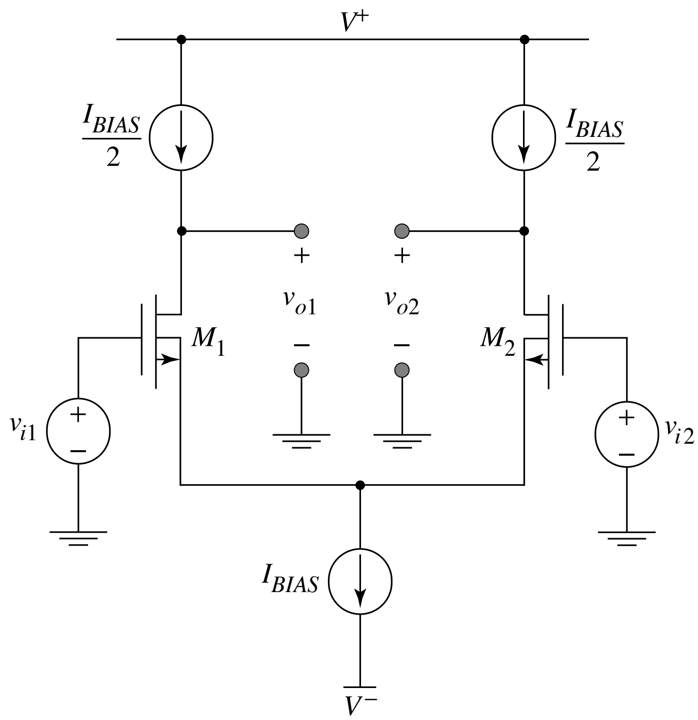
Purely differential input voltage --> $v_{o2} = -v_{od}/2 = -(1/2)a_{dm}\ v_{id}$

$$\frac{v_o}{v_{id}} = -\left(\frac{1}{2}\right)(-g_m R_C) = \frac{g_m R_C}{2}$$

Sign change (since $v_{\pi 2} = -\ v_{id}/2$) and a loss of 50% of gain

Differential Amplifier with Current Supplies

- Boost gain by using current supplies adjusted to $I_{BIAS}/2$ instead of R_C



$a_{dm} = -g_m(r_o \| r_{oc})$ for this differential amplifier

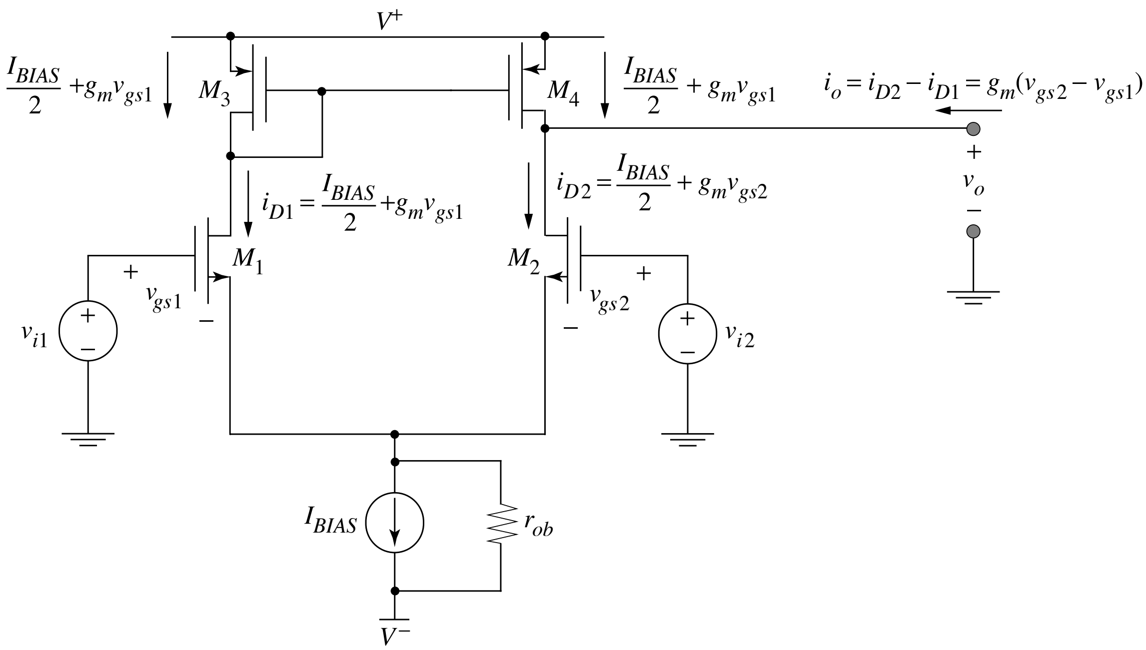
Drawbacks:

Bias stability is not possible without a feedback circuit

Taking the output from one side still reduces the gain by 50%

Differential Amplifier with Current Mirror Supply

- By substituting a current mirror (diode voltage source biasing a current source transistor), this amplifier has a stable bias



The output node should be held at a constant DC potential

$V_{OUT} = V^+ - V_{SG3}$

so that the amplifier is balanced and the output is a small-signal short-circuit

- Note that this amplifier is *not* symmetrical and that half circuits do not apply

Short-Circuit Transconductance G_{md}

- Approximate circuit analysis:

$$i_{D1} = I_{D1} + g_{m1} v_{gs1} = \frac{I_{BIAS}}{2} + g_m v_{gs1}$$

$$i_{D2} = I_{D2} + g_{m2} v_{gs2} = \frac{I_{BIAS}}{2} + g_m v_{gs2}$$

Current mirror forces the drain current $-i_{D4} = -i_{D3} = i_{D1}$

Kirchhoff's current law at the output states that

$$i_O = i_{D2} - (-i_{D4}) = i_{D2} - i_{D1}$$

$$i_O = \left(\frac{I_{BIAS}}{2} + g_m v_{gs2}\right) - \left(\frac{I_{BIAS}}{2} + g_m v_{gs1}\right) = g_m (v_{gs2} - v_{gs1})$$

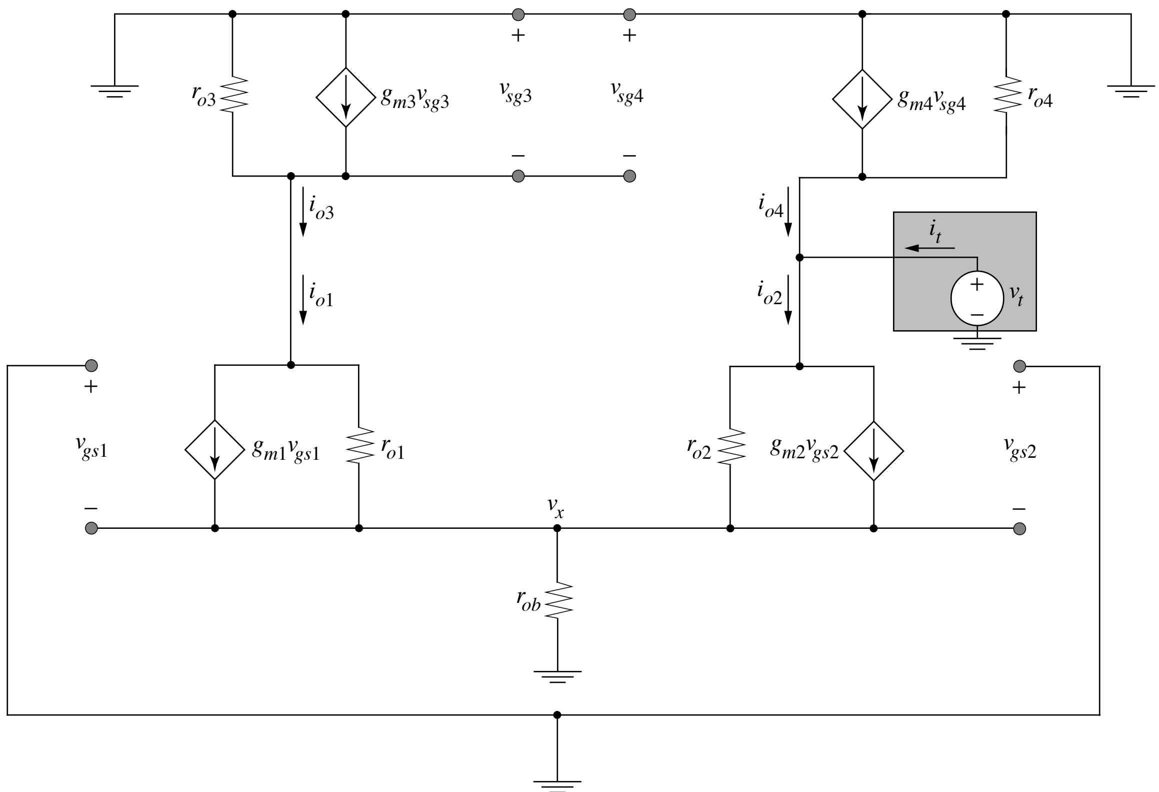
Kirchhoff's voltage law at the input states that $v_{gs2} - v_{gs1} = v_{i2} - v_{i1} = -v_{id}$

$$i_o = g_m(-v_{id}) \text{ --> } \boxed{G_{md} = \frac{i_o}{v_{id}} = -g_m}$$

- No factor of two in converting differential input into a single-ended current!

Output Resistance R_{od}

- The current-mirror circuit is not symmetrical, so the procedure must be applied to the entire amplifier

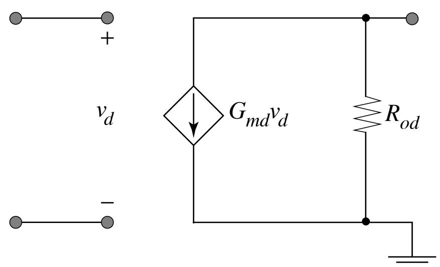


- Complicated analysis (see Section 11.5), but a simple result

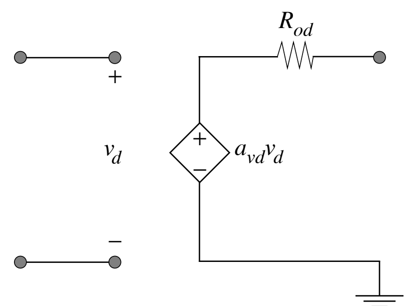
$$R_{od} = r_{o2} \| r_{o4}$$

Two-Port Differential Model: Current-Mirror Supply

- The output port is referenced to ground, in contrast to the earlier model of the symmetrical amplifier with $v_o = v_{od}$



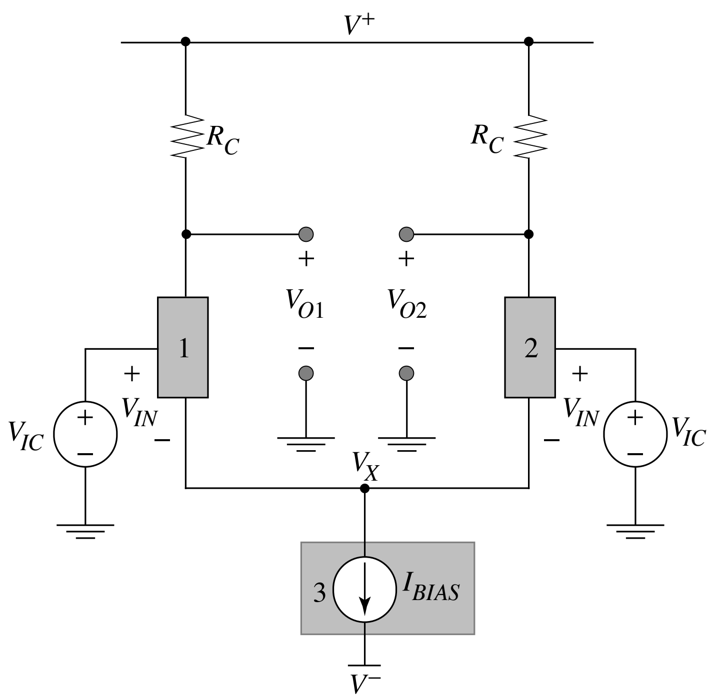
(a)



(b)

Input Common-Mode Voltage Range

- The range of DC common-mode inputs over which the differential amplifier can function is an important practical specification (see op amp spec. sheets)



Upper limit to V_{IC}

devices 1 and 2 leave their constant-current regions

Lower limit to V_{IC}

bias current device 3 leaves its constant-current region

All-Bipolar Differential Amplifier V_{IC} Range

- Maximum common-mode input voltage:

  $V_{O1} = V^+ - (I_{BIAS}/2)R_C$

  Q_1 enters saturation when $V_{BC1} = V_{BE1} - V_{CE(sat)1} = 0.7\text{ V} - 0.1\text{ V} = 0.6\text{ V}$

$$V_{IC(\max)} = V_{O1} + 0.6\text{ V} = V^+ - \left(\frac{I_{BIAS}}{2}\right)R_C + 0.6\text{ V}$$

- Minimum common-mode input voltage:

  $V_X = V_{IC} - V_{BE1} = V_{IC} - 0.7\text{ V}$

  Q_3 enters saturation when $V_X - V^- = V_{CE(sat)3} = 0.1\text{ V}$

$$V_{IC(\min)} = V_X + V_{BE1} = V^- + V_{CE(\text{sat})3} + V_{BE1} = V^- + 0.8\text{ V}$$