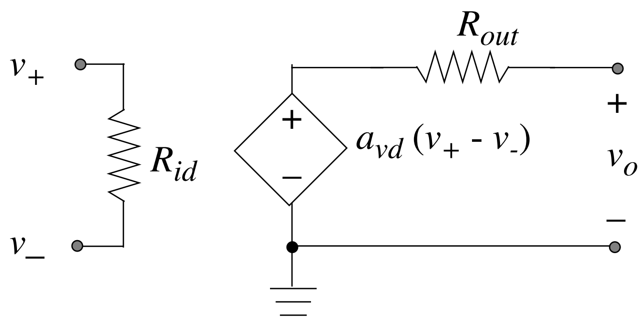
Operational Amplifiers

- Two-port (differential) small-signal model of an op amp



- Ideal "general purpose" op amp:

  R_{id} --> infinity, R_{out} --> 0, a_{vd} --> infinity

  Examples: 741 op amp has

  R_{id} = 2.7 MΩ, R_{out} = 47 Ω, a_{vd} = 300,000 (approx).

  MOS inputs --> can get near-infinite differential input resistance

- *Many* other specifications ...

  DC input common-mode voltage range and output swings

  output current sourcing (out) or sinking (in) capability

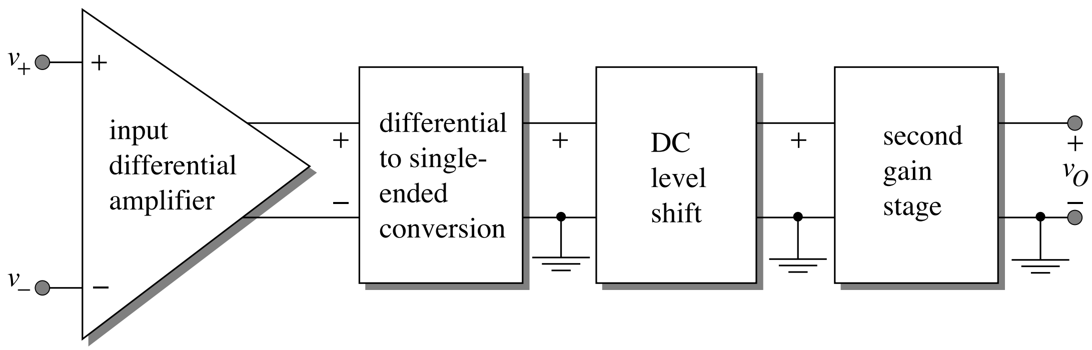
  offset voltage and its temperature dependence

Internal Op Amps

- "Internal" op amp: loads are *capacitive* --> no need for R_{out} --> 0 Ω

  therefore, *no* output stage (common-collector or common-drain)

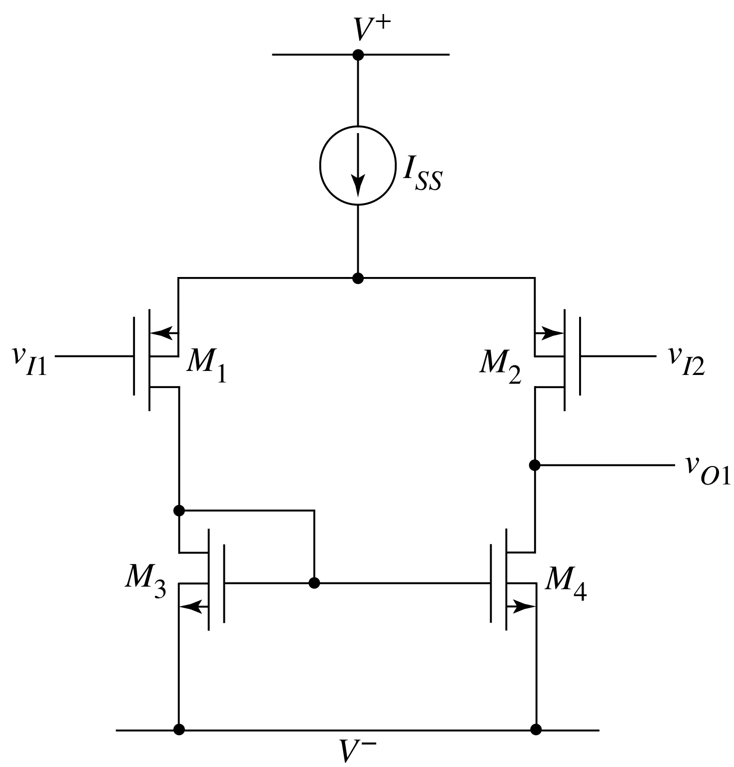
- Building block construction of an internal operational amplifier:



Differential Input Stage

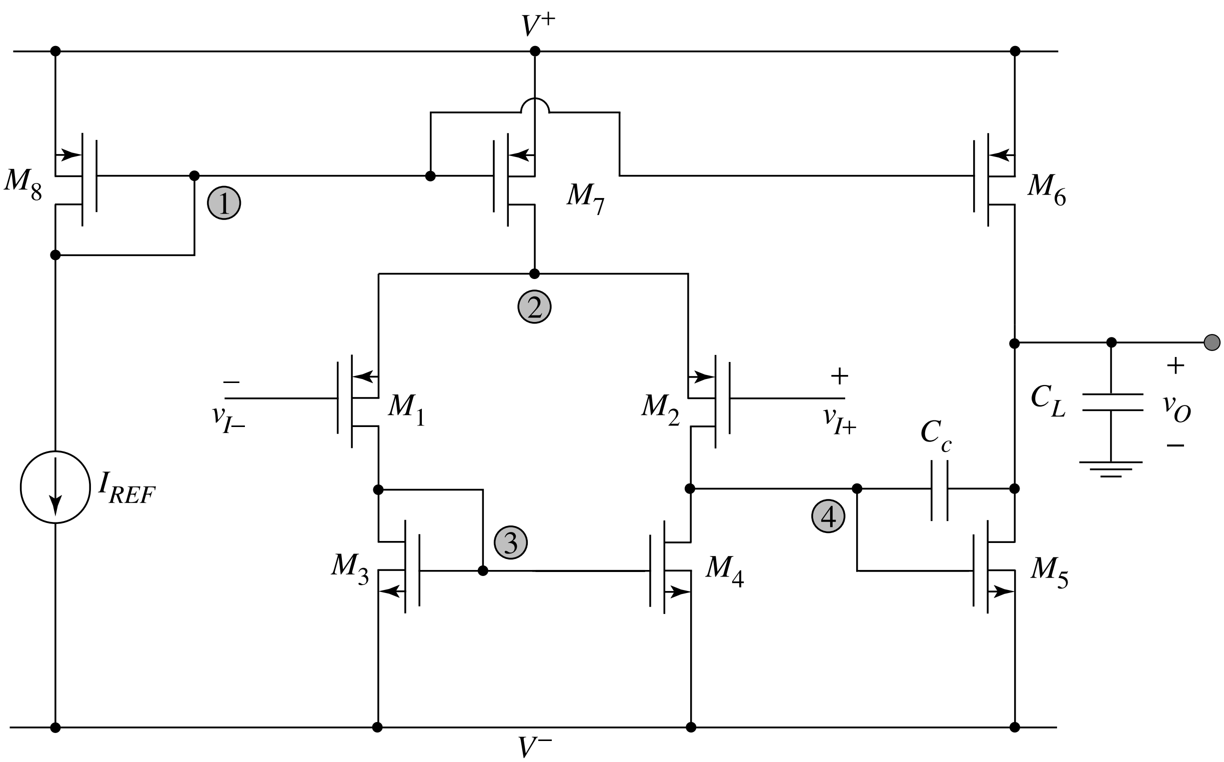
- By using a current-mirror, we can implement differential-to-single ended conversion together with the differential input stage (without loss of 3 dB gain)

  simple MOS version of input stage



Basic Two-Stage CMOS Op Amp Topology

- Add a second common-source gain stage to boost the overall voltage gain

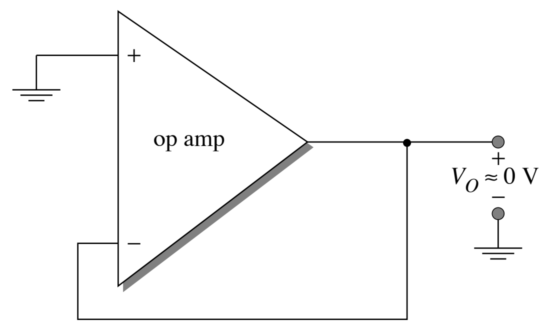


Capacitor C_c is important in the op amp frequency response

DC output is assumed to be $V_O = 0$ V

DC Bias Solution

- High gain --> place op amp in unity gain feedback loop to establish a stable DC operating point



- *Node 1*

The source-gate voltage is defined by the DC current in M_8

$$V_1 = V^+ - \left(-V_{Tp} + \sqrt{\frac{2I_{REF}}{\mu_p C_{ox}(W/L)_8}} \right)$$

- *Node 2*

The input voltages are at (nearly) zero volts, so the source-gate voltage of M_1 and M_2 determines V_2

$$V_2 = -V_{Tp} + \sqrt{\frac{2(-I_{D7}/2)}{\mu_p C_{ox}(W/L)_{1,2}}}$$

- *Node 3*

The voltage is set by diode-connected M_3

$$V_3 = V^- + V_{Tn} + \sqrt{\frac{2(-I_{D7}/2)}{\mu_n C_{ox}(W/L)_{3,4}}}$$

DC Bias Solution (Cont.)

- *Node 4*

$$V_4 = V^- + V_{Tn} + \sqrt{\frac{2(-I_{D6})}{\mu_n C_{ox}(W/L)_5}}$$

- DC voltages of drains of M_1 and M_2 should be matched to avoid a systematic offset --> $V_3 = V_4$

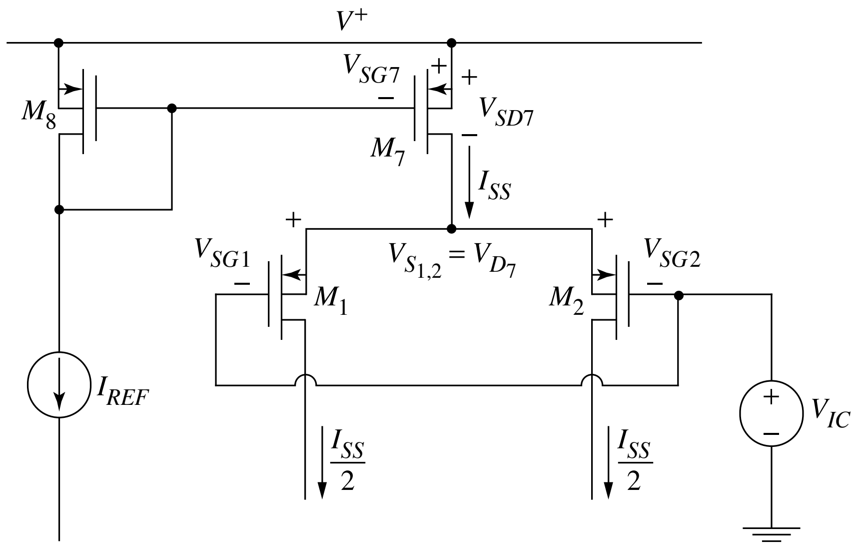
$$\sqrt{\frac{2(-I_{D7}/2)}{\mu_n C_{ox}(W/L)_{3,4}}} = \sqrt{\frac{2(-I_{D6})}{\mu_n C_{ox}(W/L)_5}}$$

$$\frac{-I_{D6}}{-I_{D7}} = \frac{(W/L)_5}{2(W/L)_{3,4}} = \frac{(W/L)_6}{(W/L)_7}$$

where the second equality follows from $V_{SG6} = V_{SG7}$

Common-Mode Input Voltage Range

- As V_{IC} increases, Node 2 follows and eventually M_7 will enter the triode region



$$V_{SD7} = V^+ - (V_{IC} + V_{SG1})$$

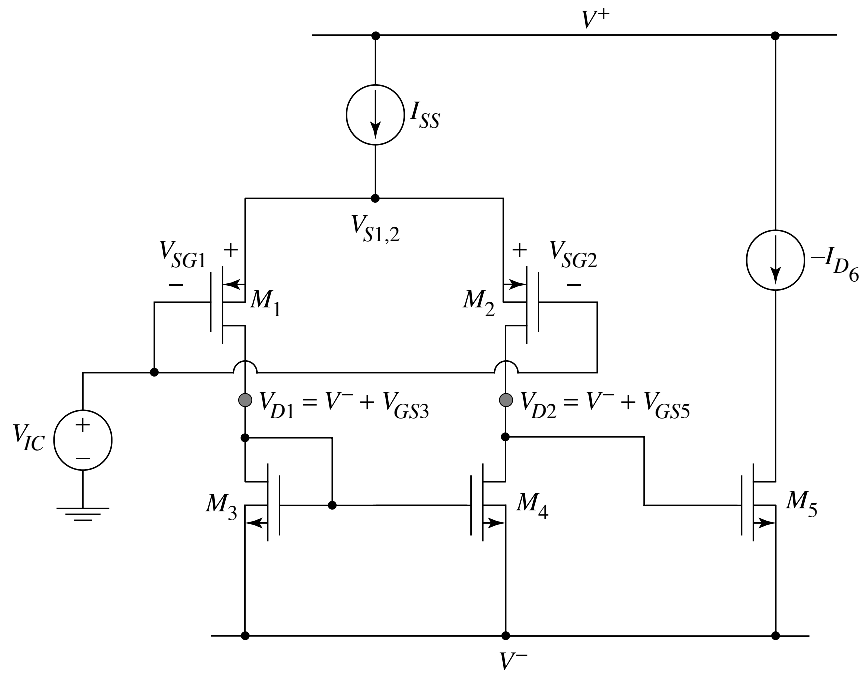
Maximum input common-mode voltage:

$$V_{SD7(sat)} = V_{SG7} + V_{Tp} = V^+ - (V_{IC,max} + V_{SG1})$$

$$V_{IC,max} = V^+ - V_{Tp} - V_{SG1} - V_{SG7}$$

Common-Mode Input Voltage Range (Cont.)

- As V_{IC} decreases, the input pair will eventually enter the triode region



$$V_{SD1} = (V_{IC} + V_{SG1}) - (V^- + V_{GS3}) \geq V_{SG1} + V_{Tp}$$

When M_1 just enters the triode region,

$$V_{IC,min} = V^- + V_{GS3} + V_{Tp} = V^- + V_{Tp} + V_{Tn} + \sqrt{\frac{2(I_{SS}/2)}{\mu_n C_{ox}(W/L)_3}}$$

Output Voltage Range

- The output node can increase until M_6 enters the triode region

$$V_{SD6} = V^{+} - V_O \geq V_{SG6} + V_{Tp}$$

so the maximum output voltage is

$$V_{O,max} = V^{+} - V_{Tp} - V_{SG6} = V^{+} - \sqrt{\frac{2(-I_{D6})}{\mu_p C_{ox}(W/L)_6}}$$

- Similarly, the output node can decrease until M_5 enters the triode region

$$V_{DS5} = V_O - V^{-} \geq V_{GS5} - V_{Tn}$$

$$V_{O,min} = V^{-} + \sqrt{\frac{2(-I_{D6})}{\mu_n C_{ox}(W/L)_5}}$$