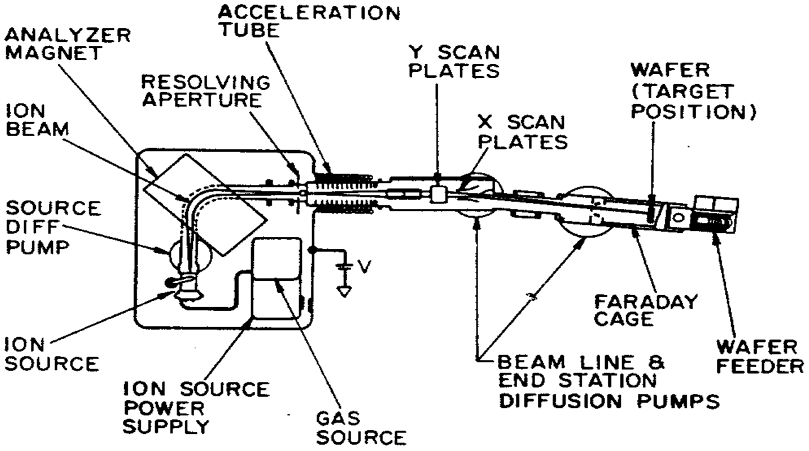
IC Fabrication Processes

- Ion Implantation

ions are accelerated to energies of 20 keV - 3 MeV and bombard the silicon wafer in a collimated beam



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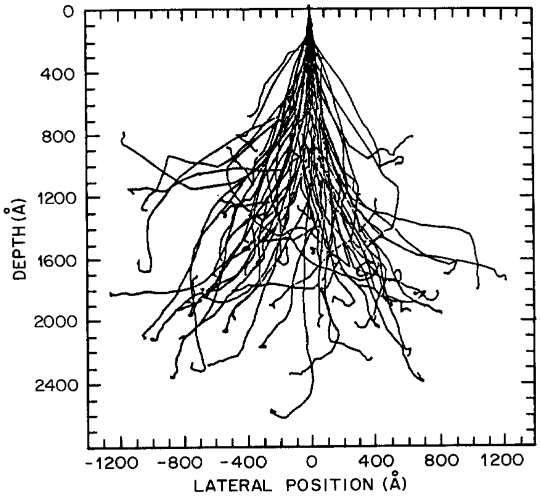
ion tracks in the silicon crystal (simulation)



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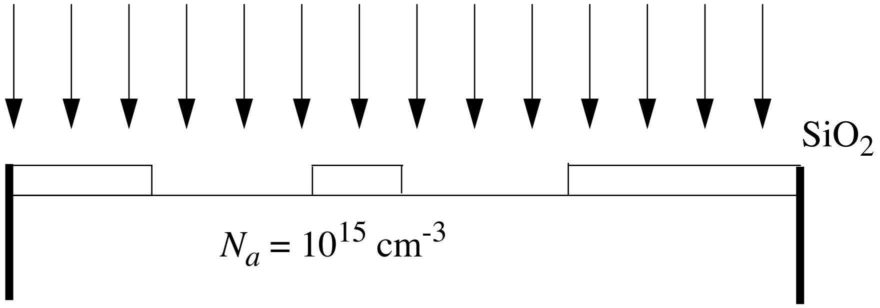
damage from implantation can be *annealed* by heating the wafer in a furnace to $T > 900$ ^{o}C.

Doping by Ion Implantation

- *Dose* = ion beam flux (# $\mathrm{cm}^{-2}\ \mathrm{s}^{-1}$) x time for implant ... units # cm^{-2}

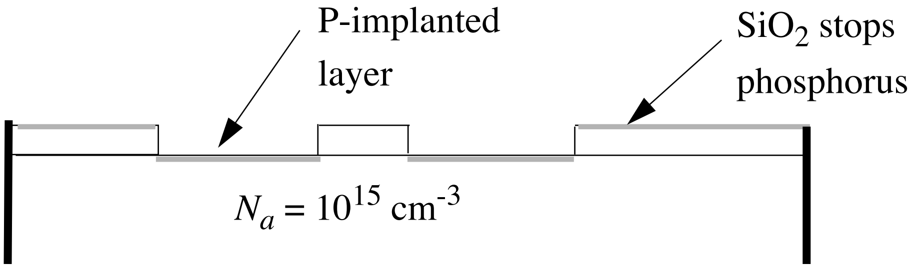
  Example:

  phosphorus ions, dose $Q_d = 10^{14}\ \mathrm{cm}^{-2}$



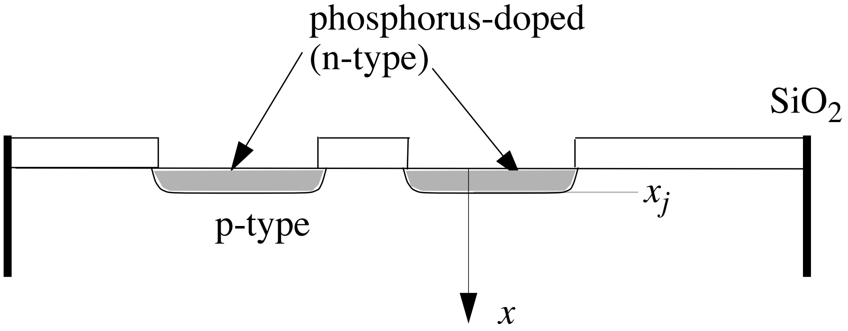
SiO_2 film masks the implant by preventing ions from reaching the underlying silicon (assuming it's thick enough)

> after implantation, the phosphorus ions are confined to a damaged region near the silicon surface :



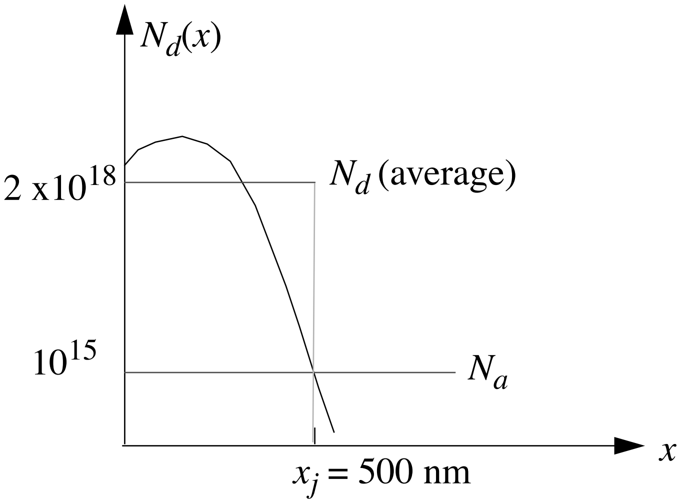
Doping by Ion Implantation (cont.)

- Annealing heals damage and also redistributes the ions (they diffuse further into the silicon crystal)



x_j is the *junction depth* and is the point where $N_d = N_a$

- Details of $N_d(x)$ ... later in an advanced course. We will use the average concentration in the n-type region for a given junction depth here.



- Average donor concentration in n-type layer = $N_d = Q_d / x_j$

IC Materials and Processes

- *Polycrystalline silicon (polysilicon)*: silicon deposited from a gas at temperatures around 600 ^{o}C, made up of small crystallites (grains), so-so conductor when heavily doped with phosphorus, but can survive very high temperatures. Useful for making micromechanical structures

- *Deposited oxides*: silicon dioxide deposited from a gas at temperatures from 425 ^{o}C to 600 ^{o}C, boron and phosphorus are sometimes added to allow it to flow. These oxides are known as “CVD” oxides for “chemical vapor deposition.”

- *Metals*: aluminum is the standard “wire” for ICs and is usually deposited by “sputtering.” Tungsten (grown from a gas reaction) is sometimes used, with increasing interest in copper.

In order to make an IC, we need

1. the mask patterns (the *layout*)

2. the sequence of fabrication steps (the *process* ... or *recipe*)

Depicting Mask Pattern Overlays

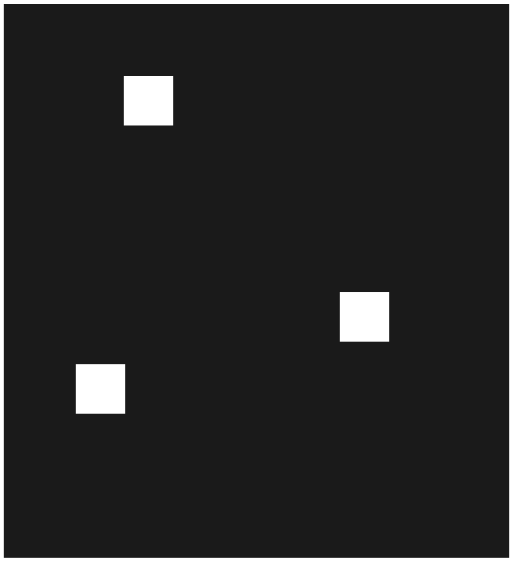
Problem: some mask plates are mostly black --> difficult to depict in the CAD layout tool since the pattern for that mask will cover underlying masks (even with high resolution color and clever “fill” patterns).

Solution: draw the negative of mostly black mask patterns in the layout editor and then label that mask carefully, so that you remember to make the inverse!

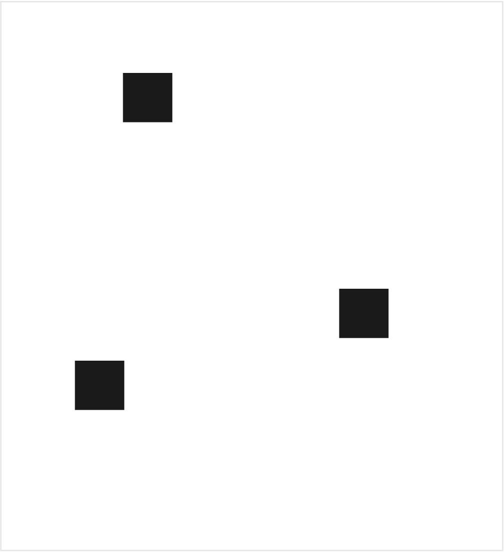
Nomenclature: “dark field” means the negative pattern is drawn
“clear field” means that the pattern is drawn

Example of a dark field mask:

actual mask plate



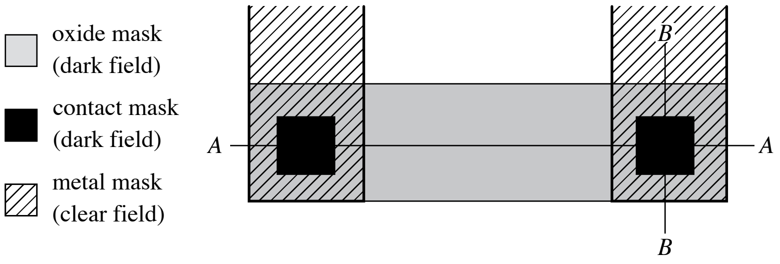
CAD layout of mask



label mask pattern “dark field”

Process Flow Examples

- Three-mask layout:



(a)

- Process (highly simplified):

1. Grow 500 nm of thermal oxide and pattern using oxide mask

2. Implant phosphorus and anneal

3. Deposit 600 nm of CVD oxide and **pattern using contact mask**

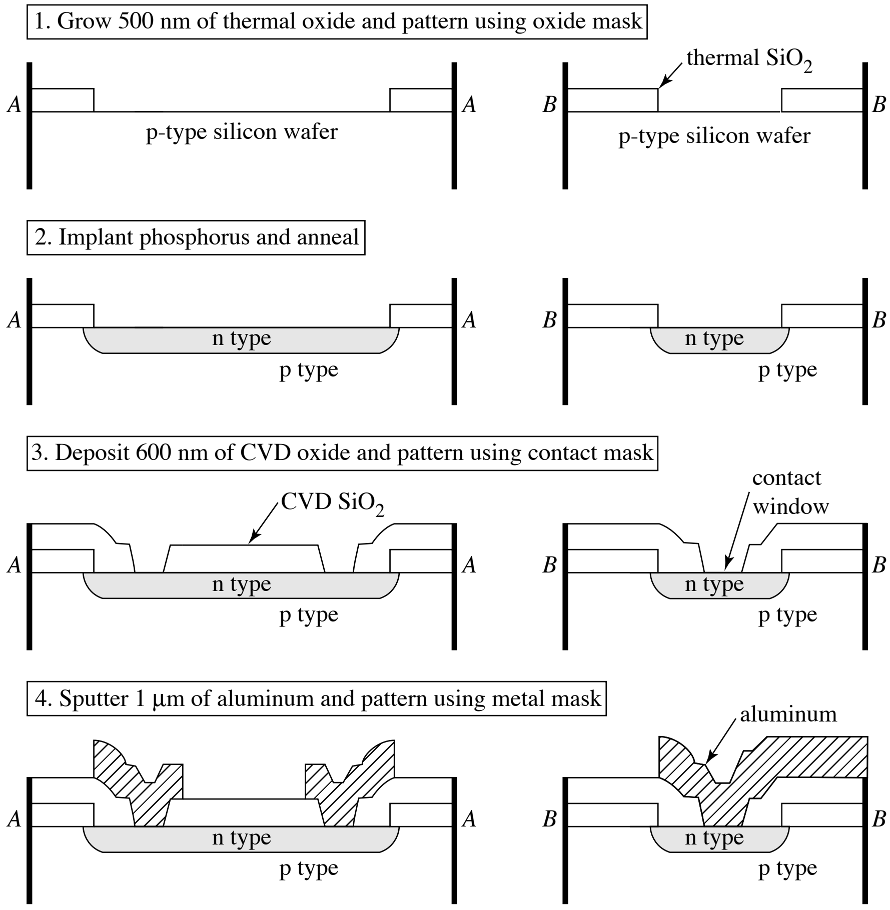
4. Sputter 1 µm of aluminum and pattern using metal mask

** note that **pattern using xxx mask** involves photolithography (including alignment to earlier patterns on the wafer), as well as etching using a plasma or “wet” chemicals, and finally, stripping photoresist and cleaning the wafer.

- 1996 IC fab: nearly 30 masking steps for some dRAM processes!

Cross Sections

- Shown on layout; only draw top few µm of the silicon wafer
- Technique: keep track of dark/light field label for each mask and be careful to be consistent on what is added or etched in each step

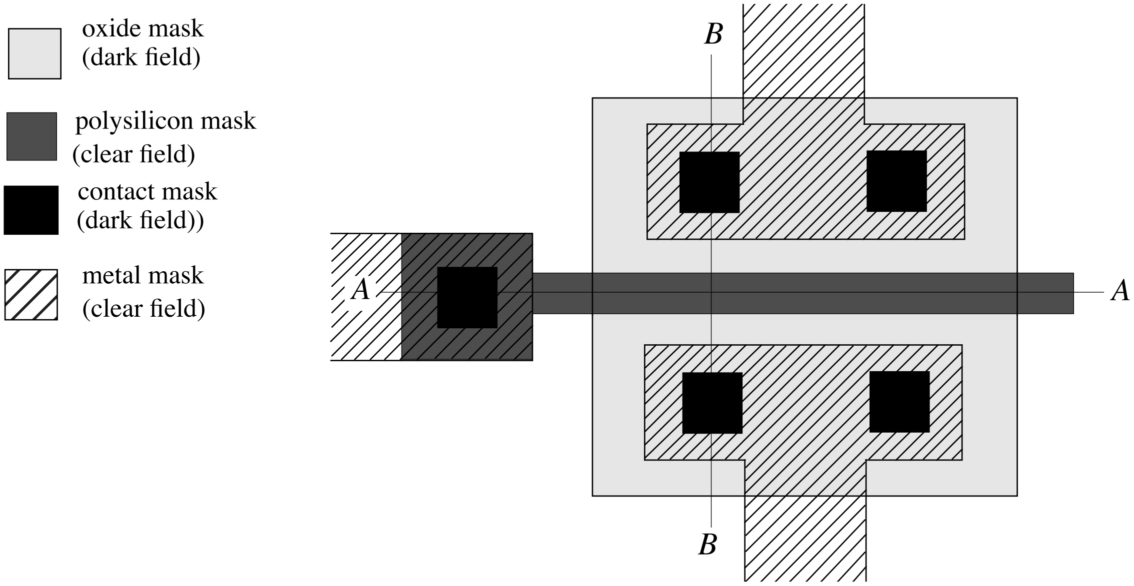


(b)

MOSFET Fabrication

- This device, the subject of Chapter 4, has made possible the revolution in digital electronics. It can be made in only 4 masking steps (one of its advantages)

- Layout



Process Flow (Simplified)

1. Grow 500 nm of thermal SiO_2 and pattern using oxide mask

2. Grow 15 nm of thermal SiO_2

3. Deposit 500 nm of CVD polysilicon and pattern using polysilicon mask

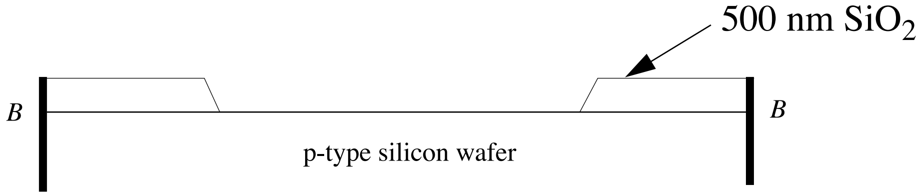
4. Implant arsenic and anneal

5. Deposit 600 nm of CVD SiO_2 and pattern using contact mask

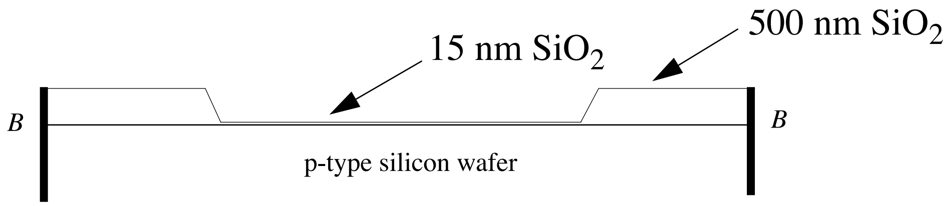
6. Sputter 1 µm of aluminum and pattern using metal mask.

- Cross sections along *B-B*

1.



2.

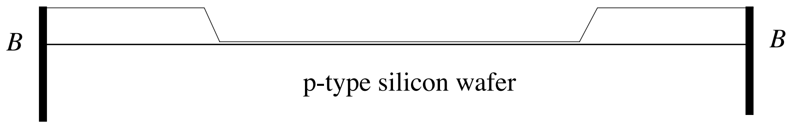


3.

MOSFET Cross Sections

- Arsenic implant/anneal, CVD oxide, and metallization steps: (incomplete)

4.



5.

6.