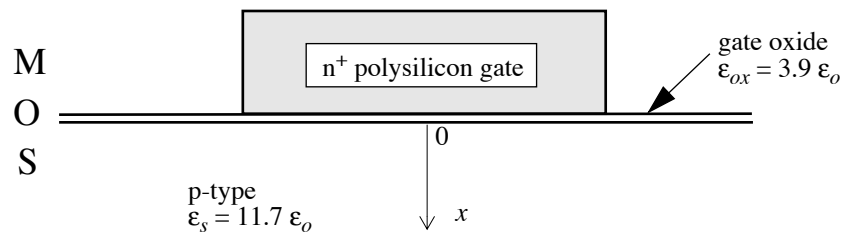


The MOS Capacitor



Oxide = SiO₂ ... a near-perfect insulator. We assume zero charge in the oxide for this course --> electric field is constant and potential is linear in the oxide.

n⁺ polysilicon has a potential which is the maximum possible in silicon:

$$\phi_{n+} = 550 \text{ mV}$$

p-type substrate has potential which is $\phi_p = -60 \text{ mV} \log(N_a / 10^{10})$

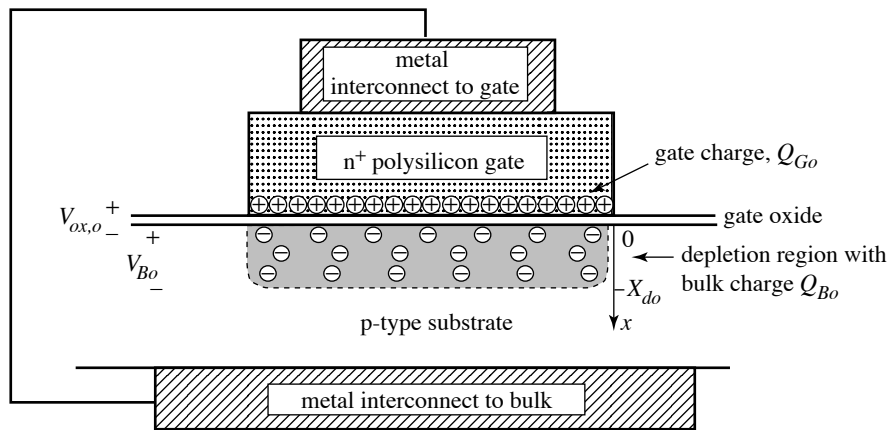
■ Strategy: same as pn junction electrostatics

first thermal equilibrium, then

with an applied bias voltage

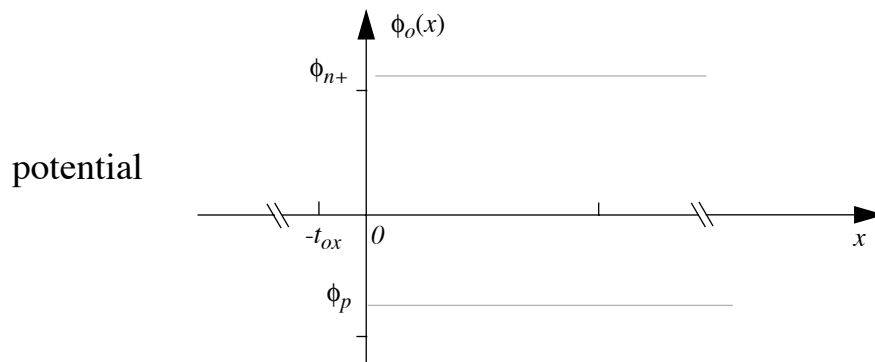
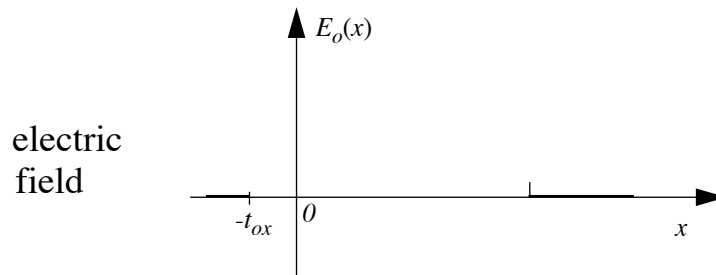
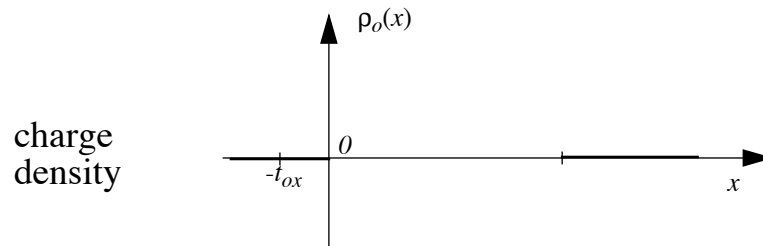
Qualitative Charge Distribution in Thermal Equilibrium

- Where to start: potential in n^+ polysilicon is known; potential in p-type substrate is known, too ... need + charge on gate, - charge in substrate --> since the silicon is p-type, this means that a depletion region forms under the gate



Thermal Equilibrium MOS Electrostatics

- Sketch charge density, electric field, and potential in equilibrium

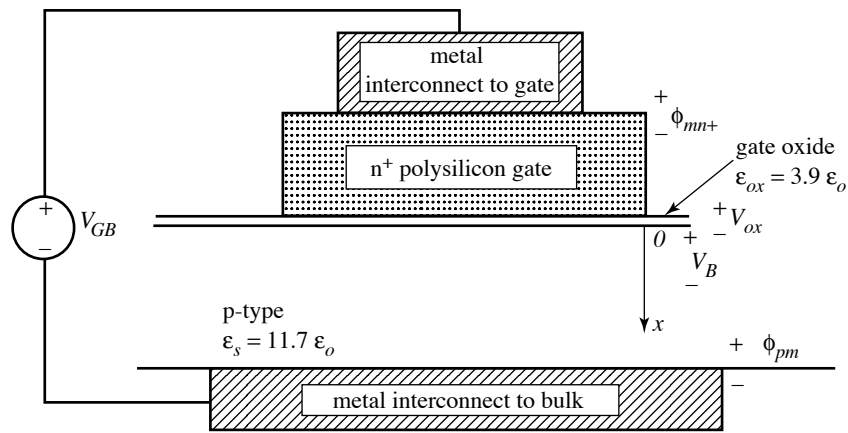


MOS Capacitor under Applied Bias

- Oxide doesn't permit any steady-state current between the n^+ poly gate and the substrate. Therefore, if we wait long enough for transient currents to die out, the electron and hole currents are zero --

$$J_n = 0 \quad \text{and} \quad J_p = 0$$

- Even though the structure isn't in equilibrium, the absence of current implies that we can relate potential to carrier concentration in the silicon substrate (since that's all we assumed in deriving the 60 mV rule.)

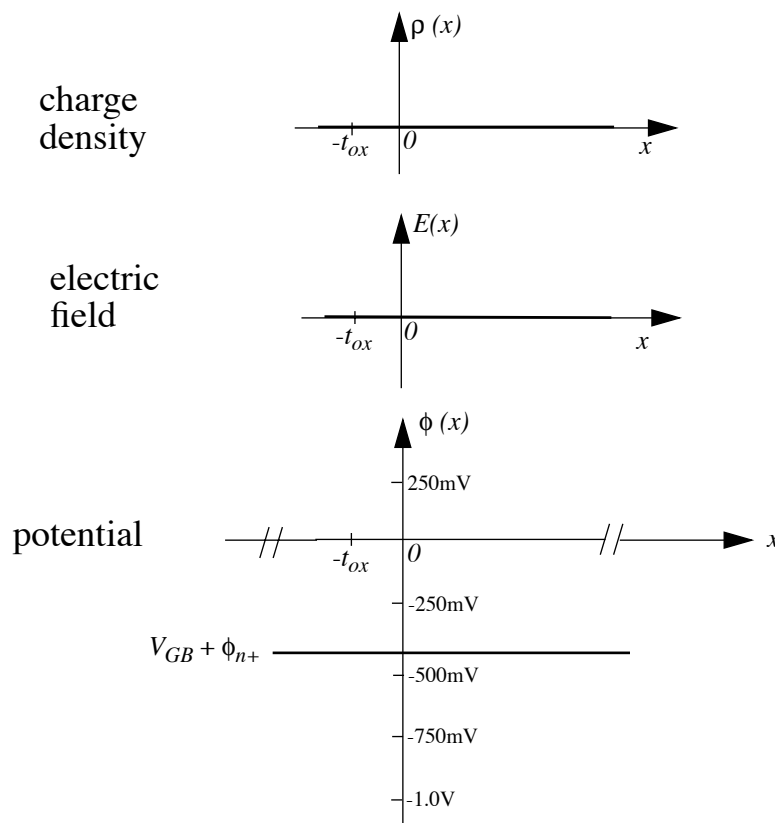


- Flatband condition: cancel built-in drop by applying the *flatband voltage*

$$V_{GB} = -(\phi_{n+} - \phi_p) = V_{FB} = -970 \text{ mV for } N_a = 10^{17} \text{ cm}^{-3}$$

MOS Electrostatics in Flatband

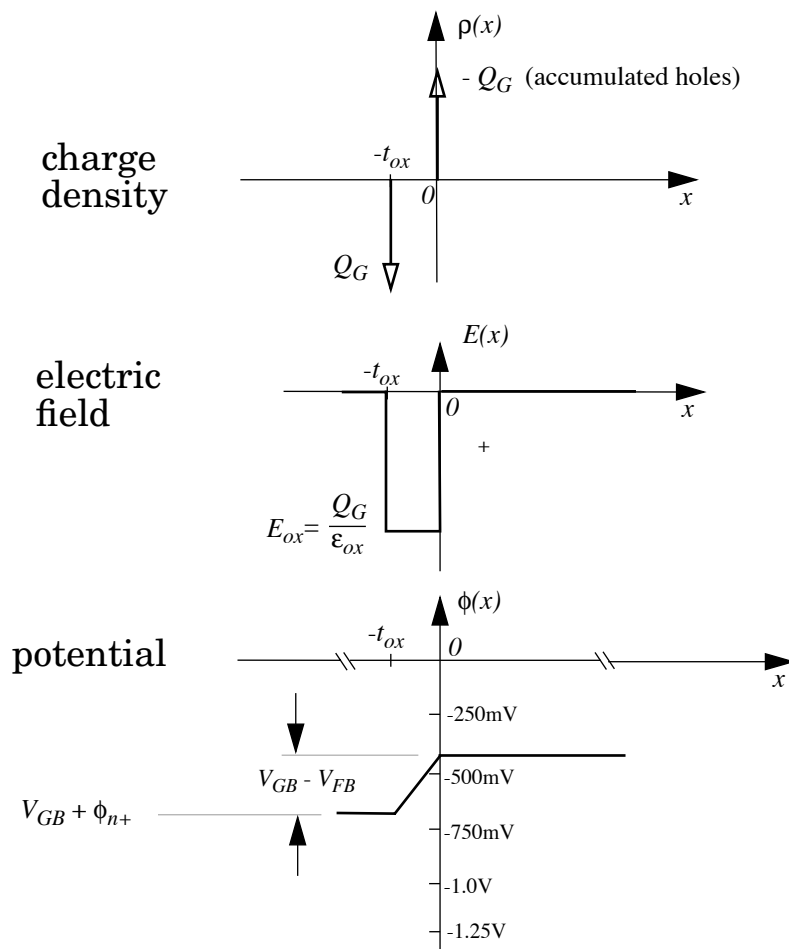
- When $V_{GB} = V_{FB}$, the gate is shifted from its thermal equilibrium potential (ϕ_{n+}) to a new value of $V_{FB} + \phi_{n+} = -(\phi_{n+} - \phi_p) + \phi_{n+} = \phi_p$, which is the same potential as the p-type bulk. Therefore, there is no potential drop across the MOS structure in flatband



- If we continue to make the gate-bulk voltage more negative, the gate will take on a negative charge $Q_G < 0$. The substrate has a positive charge, which comes from holes that are attracted by the negative gate charge

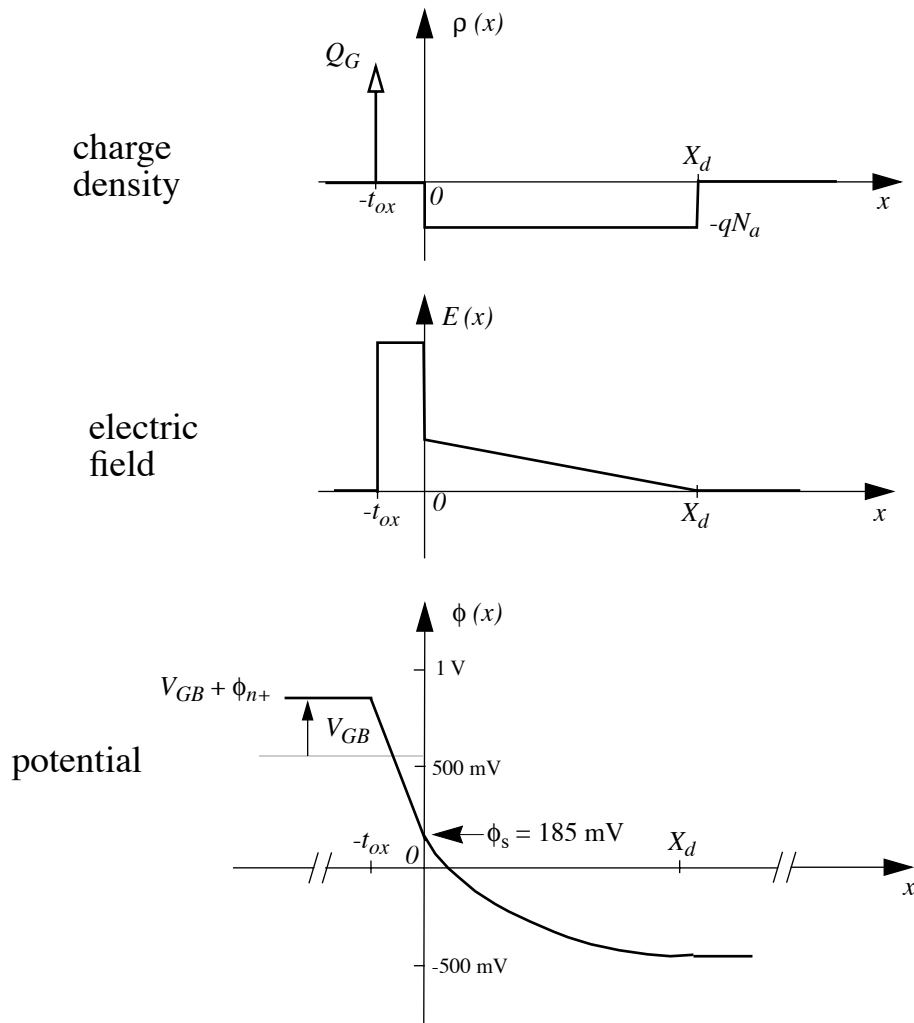
MOS Capacitor in Accumulation

- Charge density, electric field, and potential in accumulation:
 $V_{GB} < V_{FB}$, where $V_{FB} = -0.97$ V for this example.



MOS Capacitor in Depletion

- Now we make $V_{GB} > V_{FB}$. Note that thermal equilibrium falls into this range of applied bias.



- Surface potential at oxide/silicon interface is now positive --> n-type (slightly, $n_s = 10^{13} \text{ cm}^{-3}$).

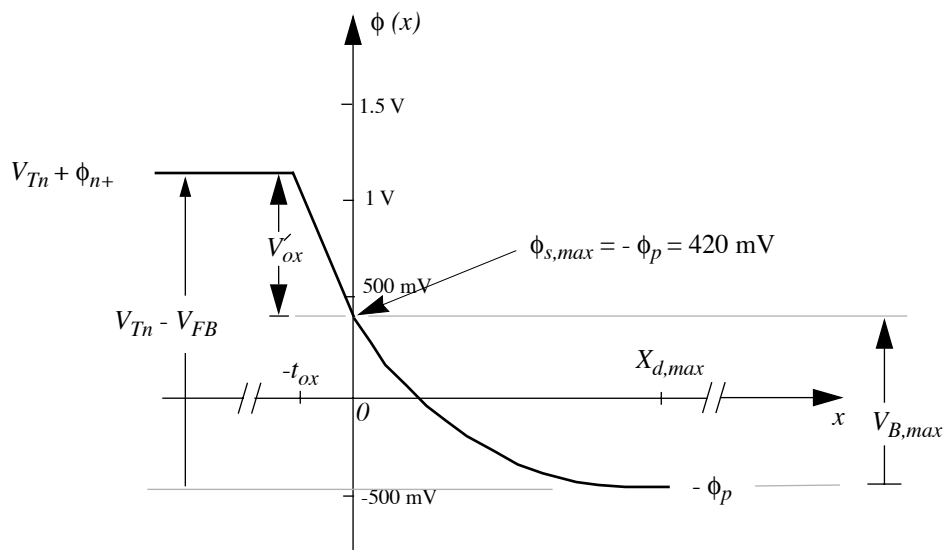
The Threshold Voltage V_{Tn}

- Keep increasing V_{GB} --> surface potential keeps increasing. At some point, the surface is n-type (i.e., we say that it is *inverted*) and the electron charge makes a significant contribution to the charge density.

How do we model this phenomenon? We approximate that onset of inversion as the point where the electron concentration n_s at the surface is the same as the hole concentration N_a in the bulk. (In other words, “the surface is as n-type as the bulk is p-type.”)

The gate-bulk potential at the onset of inversion is called the *threshold voltage*, V_{Tn} . To find the threshold voltage, we need to consider the electrostatics in depletion (no electrons at the surface at the onset of inversion) -- with the surface potential equal to the opposite of the bulk potential:

$$\phi_{s, max} = -\phi_p$$



Threshold Voltage Expression

- We can solve for the threshold voltage:

$$V_T - V_{FB} = V_{ox}' + V_{B,max}$$

- The drop across the depletion region is

$$V_{B,max} = \phi_{s,max} - \phi_p = -\phi_p - \phi_p = -2\phi_p$$

- The drop across the oxide for $V_{GB} = V_{Tn}$ is

$$V_{ox}' = E_{ox}' t_{ox} = \left(\frac{-Q_{B,max}}{\epsilon_{ox}} \right) t_{ox} = \frac{-Q_{B,max}}{C_{ox}}$$

- The bulk charge in inversion is found from the depletion width $X_{d,max}$

$$Q_{B,max} = -qN_a X_{d,max} = -qN_a \sqrt{\frac{-2\phi_p}{((1/2)qN_a)/\epsilon_s}} = -\sqrt{2q\epsilon_s N_a (-2\phi_p)}$$

where the relationship between the depletion width $X_{d,max}$ and the drop across the depletion region $\phi_{s,max} - (\phi_p) = -\phi_p - \phi_p = -2\phi_p$ can be found from Poisson's Equation.

Threshold Voltage (p-type Substrate)

- The threshold voltage is the sum of the flatband voltage (which cancels the built-in potential drop from gate to bulk), the drop across the oxide at the onset of inversion, and the maximum potential drop across the depletion region

$$V_{Tn} = V_{FB} - 2\phi_p + \frac{1}{C_{ox}} \sqrt{2q\epsilon_s N_a (-2\phi_p)}$$