Experiment 10 - Multistage Amplifiers

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UC Berkeley EE 105

1.0 Objective

In Exps. 8 and 9, you found the small signal properties of single stage amplifiers (e.g., Common Emitter, Common Collector, Common Drain, etc.) Now you will see how these single stage amplifiers perform together. By cascading the single stage devices, new amplifiers with enhanced performance can be realized. You will also study the effects of loading between stages.

To show your understanding of the lab, your write-up should contain:

- A discussion on how single stages interact together
- A discussion on interstage loading based on 2-port models

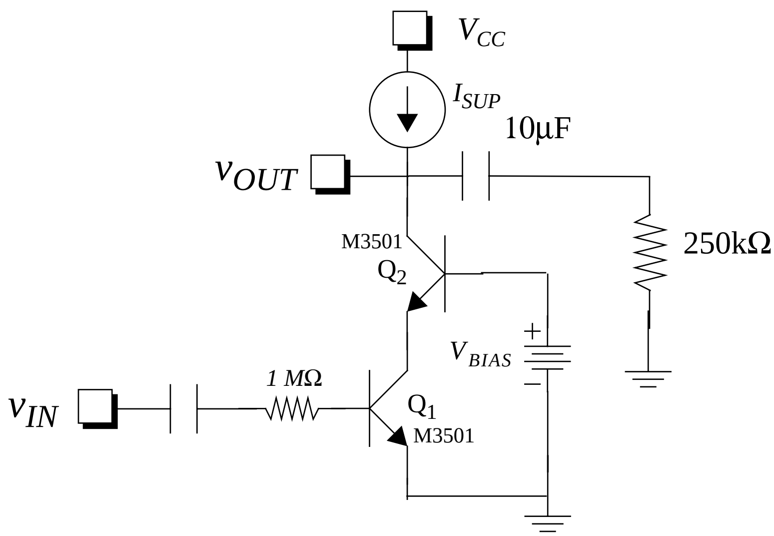
2.0 Prelab

- H & S: Chapter 9
- For the Cascode Circuit in figure 1, calculate the gain, input resistance and output resistance for a supply current of I_{SUP} = 1 mA.

  (Use npn: β_n = 80, V_{An} = 50 V, - pnp: β_p = 30, V_{Ap} =15 V.)

  Given: the current-source supply in figure 1 has a small-signal resistance $r_{oc} = \beta_p r_{op}$.

FIGURE 1. Cascode Amplifier with Current Source Supply



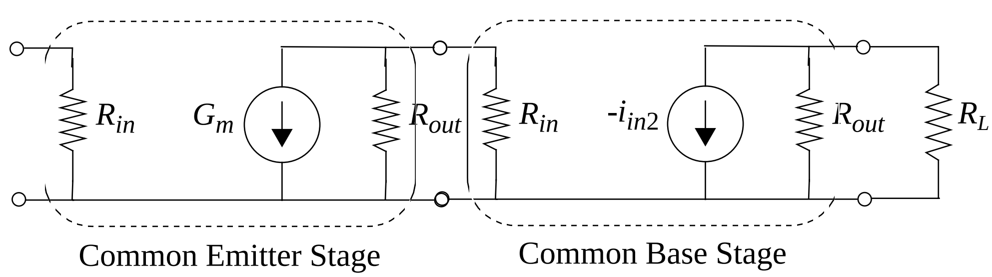
3.0 Procedure

3.1 The Cascode

The Cascode circuit is nothing more than a Common Emitter - Common Base (or Common Source - Common Gate) cascade. Figure 1 above shows a simplified cascode with a current source load.

The 2 port model for the cascode is shown below

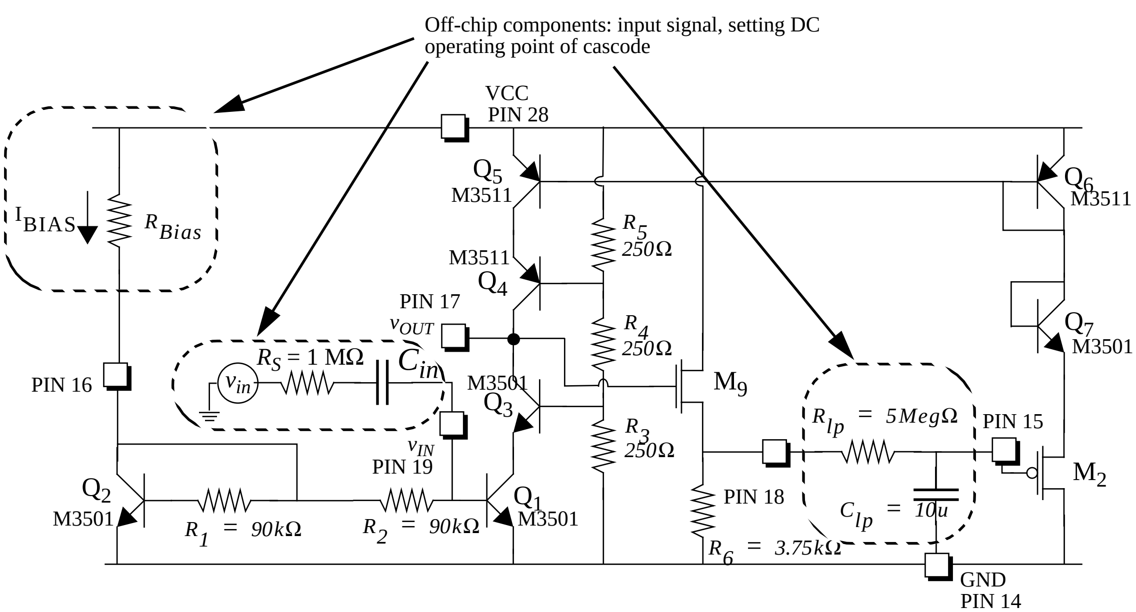
FIGURE 2. 2-Port Representation of Cascode



In your lab, the cascode circuit will include extra biasing circuits as shown in figure 3. These circuits make use of DC feedback (coupled through the external low-pass filter), in order to stabilize this high-gain circuit. After simplification, figure 3 reduces to the basic cascode amplifier in figure 1.

1. Set up the circuit from Lab Chip 4 as shown in figure 3. Let R_{Bias} be 10 kΩ and C_{in} be 10 μF. Let V_{CC} be set at 5V. Note: The user just needs to furnish the external elements in the box. (the elements in the dashed "boxes" in figure 3).
2. Determine the bias current and DC voltage at V_{OUT}. Using figure 3, what are the maximum and minimum DC voltages that V_{OUT} can swing to while keeping all the devices in the forward active region. Compare with measurements of output clipping levels.
3. Using the oscilloscope, find the gain v_{out}/v_{in}. Use a 5 kHz sine wave with an amplitude of 200 mV. If the signal at the output is clipped, decrease the input amplitude until no clipping occurs.
4. *Calculate* the input resistance and output resistance for the cascode. Using the calculated value of the input resistance, you can calculate how much of the input voltage is attenuated. Determine the gain of the cascode v_{out}/v_{in}. How does the cascode compare to the Common Emitter in terms of input resistance, output resistance and voltage gain? Optional: *measure* the input and the output resistances.

FIGURE 3. Bipolar Cascode with DC Feedback Biasing (Lab Chip 4)



Lab Tip

Find the DC voltage at v_{OUT} (PIN 17) and make sure that Q_3 and Q_4 are not saturated. If they are, get a new chip.The circuit takes about 10 - 20 seconds to stabilize. Be patient.

5. Perform a SPICE analysis on the Cascode in figure 1 (figure 3 is extra credit) and compare your results with simulation.

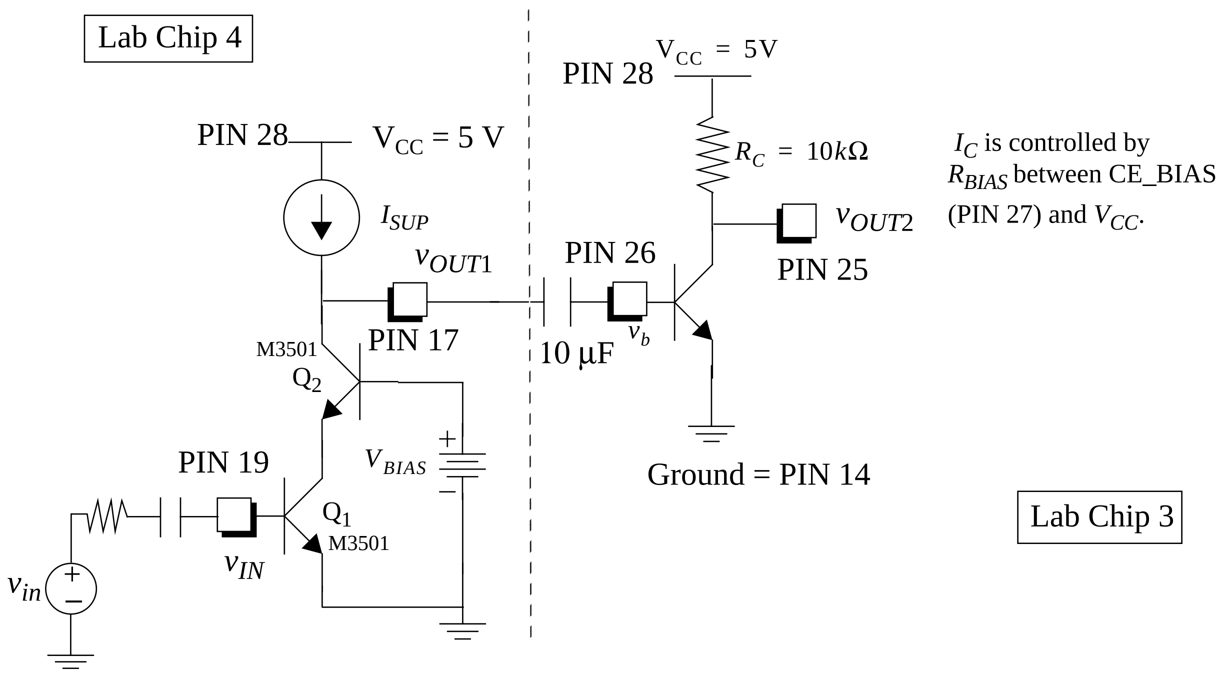
3.2 Cascading Stages

1. While leaving the Cascode intact, build the common emitter as shown in figure 4. Set R_{BIAS}(CEBIASP) to be a potentiometer and adjust it until the output is at 2.5V. (This is merely the same procedure as the common emitter circuit in Exp. 8.) Find the bias current through R_{BIAS}. Does the DC voltage at V_{OUT} confirm the fact that $I_C = I_{BIAS}$? Find the gain of the Common Emitter.

2. Now cascade the two stages together with the use of the 10 μF coupling capacitor. What is its function? (Hint: look at the DC voltage at both sides of the capacitor) What would happen if the capacitor were not present? Change the amplitude of the sinusoid to 50 mV.

3. Find the gain for the cascade. Measure the gain v_{out1} / v_{in}. Why is it reduced?

FIGURE 4. Cascode - Common Emitter Cascade



4. Draw the 2 port models for the cascaded amplifier in Fig. 4. Comment on the overall gain and the loading between stages.

4.0 Optional Experiments

4.1 Common Collector as a Buffering Stage

1. Leaving the cascode and common emitter circuit intact, we now insert a Common Collector as an intermediate stage between the Cascode and Common Emitter. Find the gain of this new circuit. For the Common Collector, set R_{BIAS} = 100 kΩ. For measuring input attenuation, the source resistance may have to be increased over the value in figure 3. Lower the amplitude of the input sinusoid and reduce the source resistance as necessary to avoid clipping at the output.
2. Draw the 2-port models for this Cascode-CC-CE configuration. Comment on the gain and the interstage loading.

FIGURE 5. Common Collector (Emitter Follower) Voltage Buffer (Lab Chip 4)