
Experiment 5 - Inverter Characteristics

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1.0 Objective

In this experiment, you will determine the *voltage transfer characteristic* (VTC) of several different MOS inverter topologies by graphing load lines and by performing actual measurements. In addition, you will be calculating and measuring the voltage gain and comparing the propagation delays of the different inverters. The key concepts introduced in this laboratory are:

- Using loadline method to find the VTC
- Comparison of different Inverter topologies
- Comparison of propagation delays for different Inverter topologies
- Comparison of voltage gains for different Inverter topologies

2.0 Prelab

- H & S: Chapters 5.1 - 5.4
- Using the I - V characteristics for NMOS ($W = 46.5 \mu\text{m}$ $L = 1.5 \mu\text{m}$) in Experiment 4, draw in the loadline for a $5 \text{ k}\Omega$ resistor. Using loadline analysis, determine the voltage transfer characteristic of this inverter.
- Using SPICE, determine the VTC for the CMOS inverter shown in figure 2a. Use the parameters from Experiment 4. You should use a graphical (loadline) approach.

3.0 Procedure

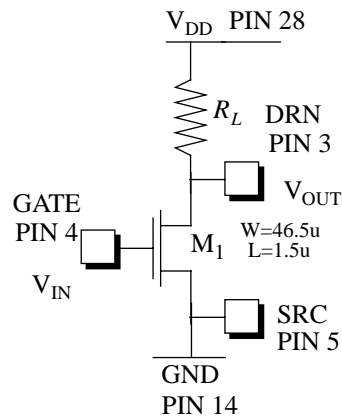
3.1 Resistively-loaded NMOS Inverter

1. Connect the NMOS inverter shown in figure 1. Let $R_L=1\text{ k}\Omega$. Don't forget to short the source (pin 5) to ground (pin 14).

FIGURE 1.

Resistively loaded NMOS inverter. The NMOS is found on Lab Chip 1.

Lab Chip 1



2. Using the DC power supply, vary the input voltage from 0 to 5 V and use the digital multimeter to determine the voltage at the output. Sketch the *voltage transfer characteristic* from the data. Comment on the important points of the graph such as V_{OH} , V_{OL} , V_M , noise margins, etc.
3. From the slope of the transition region, determine the voltage gain A_v . How does it compare with the theoretical value?
4. Attach a load capacitance of 100 nF to the output node. Apply a 200 Hz 0 to 5 volt square wave to the input of the inverter. Set the DC offset to be 2.5V. Use the oscilloscope to plot v_{IN} and v_{OUT} . Measure the propagation delays, t_{plh} and t_{phl} of the inverter.

Lab Tip

Make sure that the DC offset on the generator is set. Adjust the frequency on the generator if the circuit cannot respond fast enough. The specification at 200 Hz is by no mean set in stone.

You can to used the *delayed-time* setting on the scope to get more accurate measurements of the propagation delay time.

5. Perform a DC analysis with SPICE to find the VTC. Perform a transient analysis to find the propagation delay. How does simulation compare with experiment?

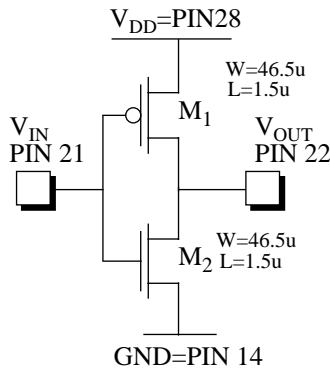
3.2 CMOS Inverter

3.2.1 DC Characteristics

1. Using the 4145, load the program **PINV**.
2. Place the Lab Chip 2 in the test fixture. Figure 2 shows the pinouts of the CMOS inverters you will be testing.

FIGURE 2.

CMOS inverter

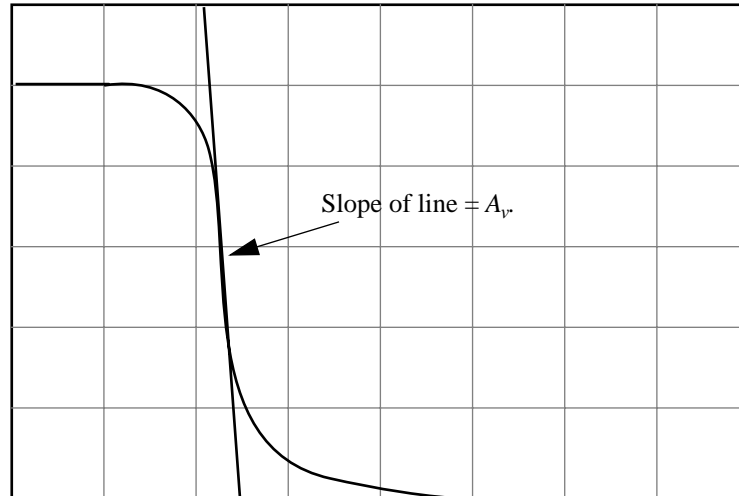


SMALL CMOS INVERTER

3. Note the channel definitions and connect the appropriate channels. In particular, connect **SMU1** to V_{in} and **VM1** to V_{out} .
4. Starting with the small CMOS inverter, perform a DC sweep by hitting the **[SINGLE]** key.
5. Note the VTC of this inverter. Using the marker and the cursor, find the slope of the line through the transition region and find the gain of the inverter. (Refer to experiment 1 if you had forgotten how to do this.)

FIGURE 3.

Sample VTC for CMOS inverter



6. Obtain a hardcopy of the VTCs. Use **[PLOT] [EXE]**.

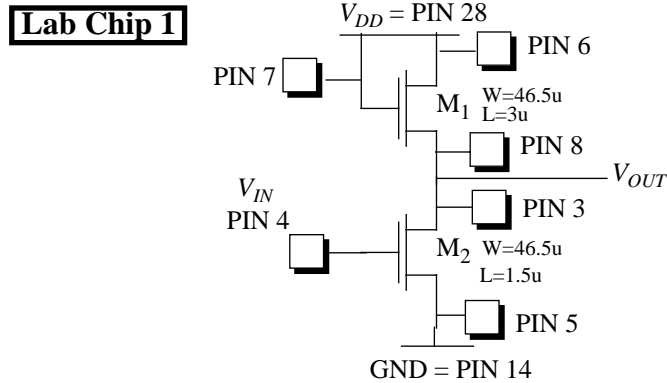
3.2.2 Transient Characteristics

1. Place the Lab chip 2 on your breadboard. Connect a 100nF capacitor at the output V_{out} .
2. Apply a 2 kHz 0 to 5 volt square wave to the input of the inverter. Set the DC offset to be 2.5V. Use the oscilloscope to plot v_{IN} and v_{OUT} . Measure the propagation delays, t_{plh} and t_{phl} , of the inverter. Also compare the delay time with the delay time of the inverter with resistive load.

4.0 Optional Experiments

4.1 Enhancement Load NMOS Inverter

FIGURE 4. Enhancement Load NMOS Inverter

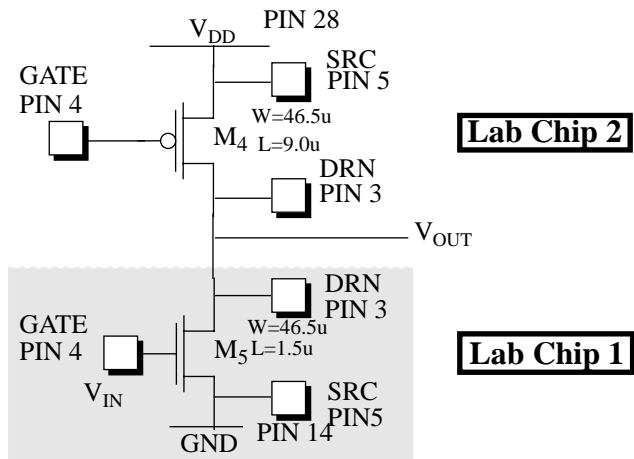


1. Place the Lab Chip 1 on your breadboard. Construct the inverter as above. Connect a 100 nF Capacitor at the output V_{OUT} .
2. Apply a 2 kHz 0 to 5 volt square wave to the input of the inverter. Set the DC offset to be 2.5 V. Use the oscilloscope to plot v_{IN} and v_{OUT} . Measure the propagation delays t_{plh} and t_{phl} of the inverter.
3. Find the propagation delays t_{plh} and t_{phl} , for this inverter. How do they compare with the others?

4.2 Pseudo NMOS Inverter

Repeat the above experiment for the following Inverter. Apply 1 volt to the gate of the PMOS. Also, apply a 500 Hz 0 to 5 volt square wave to the input of the inverter. The PMOS can be found on Lab Chip 2 while the NMOS is from Lab Chip 1.

FIGURE 5. Pseudo NMOS Inverter



5.0 Appendix

The CMOS inverter layout shown below. Note that this is the layout for the CMOS inverter in Lab Chip 2.

FIGURE 6. Layout for CMOS Inverter

