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# Experiment 6 - Digital Circuits

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## 1.0 Objective

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In this experiment, you will examine several different CMOS digital circuits. You will test the functionality of the digital logic circuits and compare the propagation delays of each. In addition, you will examine the properties of a ring oscillator. The key concepts introduced in this lab are:

- The functionality of digital circuits
- The different propagation delays associated with different transitions
- Using the ring oscillator to measure the switching speed

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## 2.0 Prelab

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- H& S: Chapter 5.5 - 5.6
- Draw CMOS circuits that implement the following Boolean equations:

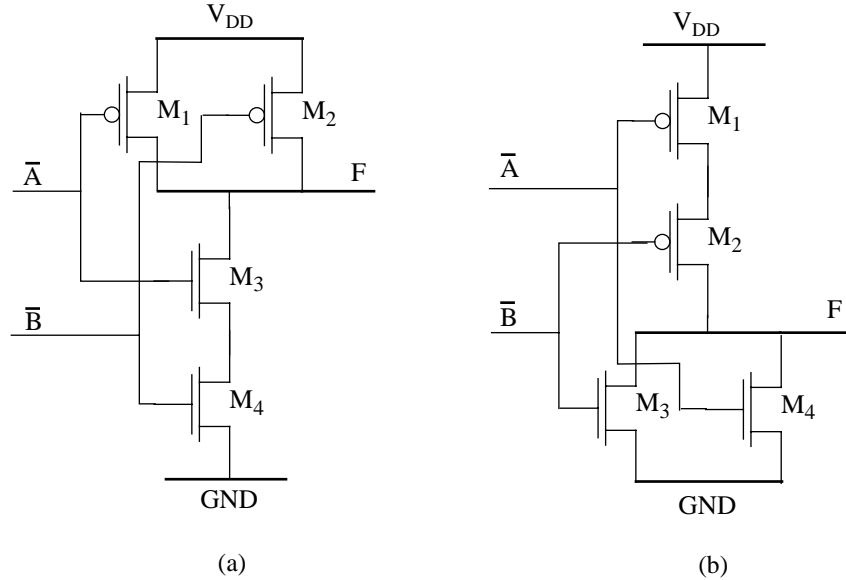
$$F=A \bullet (B+C)$$

$$F=\overline{A} \bullet \overline{B} + C$$

Write the Boolean equations and the truth tables for the circuits in figure1. What logic functions do they implement?

FIGURE 1.

CMOS Digital Circuits



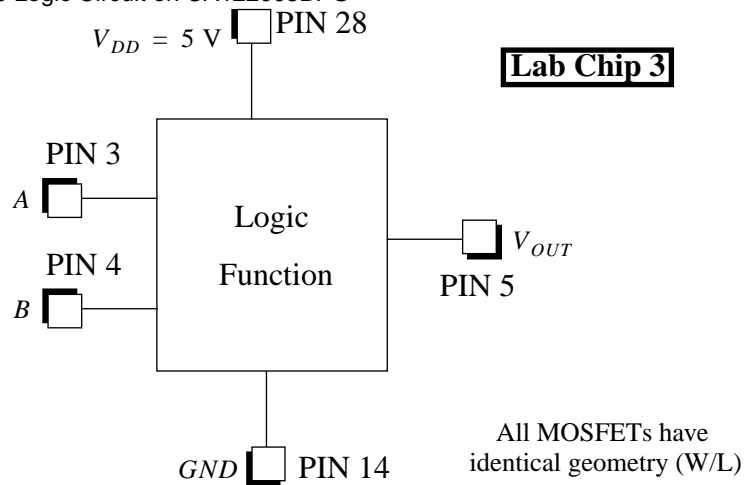
### 3.0 Procedure

#### 3.1 Determination of Logic

1. The figure below shows a “mystery” 2 input logic function on Lab Chip 3. Place the chip in your breadboard and connect the power and ground pin.

FIGURE 2.

Unknown CMOS Logic Circuit on CA122005BPG



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## Procedure

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- Construct the truth table for this circuit using all possible combinations for  $A$  and  $B$ .

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### Lab Tip

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Use the Buslines for  $GND$  and  $V_{DD}$  for the inputs  $A$  and  $B$ . This will minimize the number of wires and cables on your board.

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- Write down the Boolean equation which describes the function of the circuit. What does this circuit do?
- Place a 100 nF load on the output. Connect inputs  $A$  and  $B$  together. Connect a 0 to 5 volt square wave with a frequency of 1 kHz to the combined input. Measure  $t_{plh}$  and  $t_{phl}$ . Disconnect input  $B$  from  $A$  and connect it to ground. Measure  $t_{phl}$  and  $t_{plh}$ . Are there any differences in the delay times? What explanations can you offer?

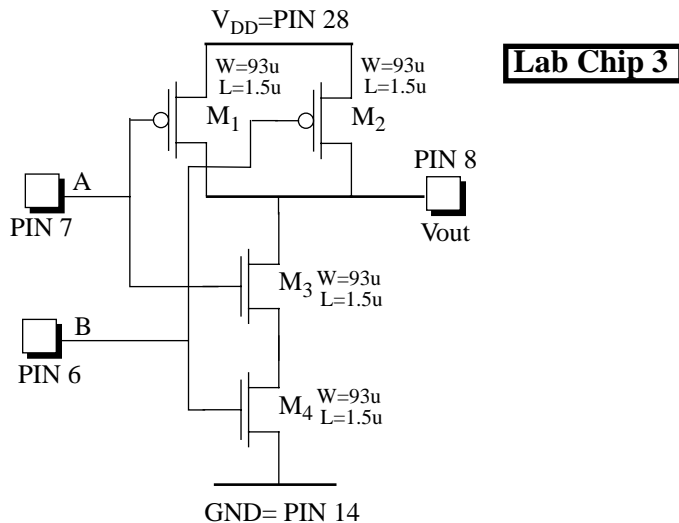
### 3.2 NAND gate

- Connect the NAND gate shown in figure 3. The NAND gate is found on Lab chip 3.

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FIGURE 3.

NAND Gate on Lab Chip 3



- Construct the truth table for this circuit using all possible combinations for  $A$  and  $B$ .
- Write down the Boolean equation which describes the NAND gate. Does the circuit perform the required function?
- Place a 100 nF load on the output. Connect inputs  $A$  and  $B$  together. Connect a 0 to 5 volt square wave with a frequency of 1 kHz to the combined input. Measure  $t_{plh}$  and  $t_{phl}$ . Disconnect input  $B$  from  $A$  and connect it to 5 volts. Measure  $t_{phl}$  and  $t_{plh}$ . Now

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## Procedure

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connect  $A$  to 5 volts and have  $B$  switch from 0 to 5 volts. Measure  $t_{phl}$  and  $t_{plh}$ . Are there any differences in the delay times? What explanations can you offer?

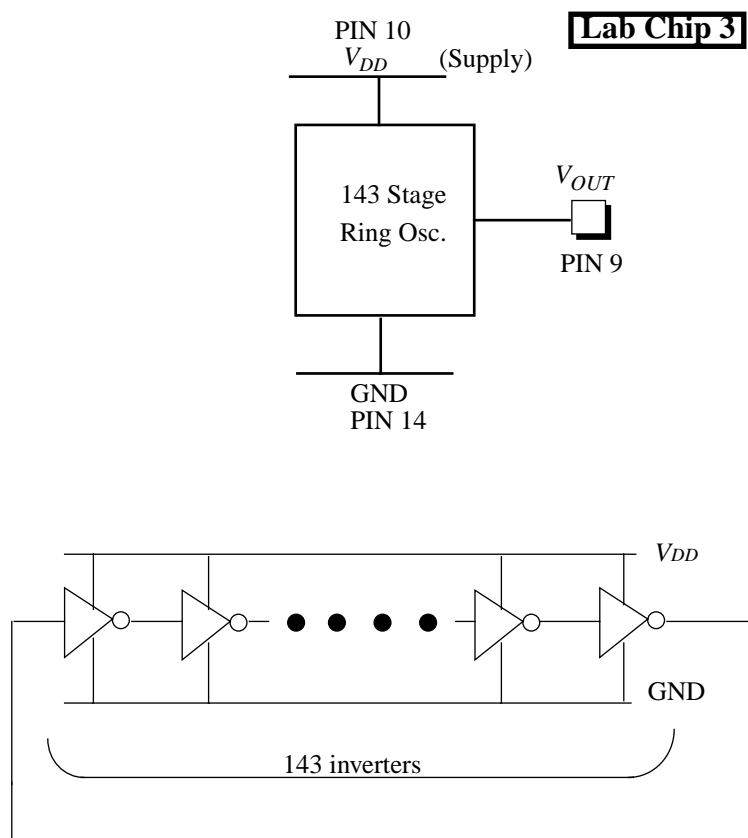
### 3.3 143 Stage Ring Oscillator

1. Connect the ring oscillator as shown below. The ring oscillator is found on Lab Chip 3. Note that the ring oscillator has its own supply pin (PIN 10).

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FIGURE 4.

Ring Oscillator Circuit



Connecting pins 28 and 10 together makes for a cleaner measurement. Vary the supply from 0 to 5 volts and measure the frequency vs.  $V_{DD}$ . Make a graph of the frequency versus the supply voltage. What sort of dependence does it have? Determine the switching speed of each inverter from the basic relationship between  $t_p$ , the number of inverters, and the frequency of the ring oscillator. Also, determine the load capacitance per stage using the value of  $K_n$  found before.

## 4.0 Optional Experiment

### 4.1 Dynamic Logic

1. Connect the dynamic logic circuit shown in figure 5. Use the DIP switch for the four inputs. Attach a load capacitance of 10 pF to the output node.
2. Write  $V_{out}$  as a function of  $A$ ,  $B$ ,  $C$  and  $\Phi$ . Connect all four inputs to switches. Normally,  $\Phi$  is connected to a clock, but in this lab you will clock the circuit manually. In precharge mode  $\Phi=0$  (0V) and in evaluate mode  $\Phi=1$  (5V). Change the logic levels of  $A$ ,  $B$  and  $C$  and check if the voltage at  $V_{OUT}$  is changing. Why shouldn't it change?
3. Let  $A=0$ ,  $B=1$  and  $C=0$  -- in evaluate mode, switch  $\Phi$  must be set to high first. If the output has a path to ground it will pull low. Check this by switching  $A$  high.

FIGURE 5.

Dynamic Logic Circuit found on Lab Chip 3

