Experiment 8 - Single Stage Amplifiers with Passive Loads - BJT

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1.0 Objective

A typical integrated circuit contains a large number of transistors that perform many functions. The simplest way to analyze such a circuit is to regard each individual transistor as a stage and to analyze the circuit as a collection of single transistor stages. In this experiment, you will examine the behavior of some single-stage amplifiers with resistors supplying the bias current. You will measure properties such as voltage gain, input impedance and output impedance. From these measurements you should understand the relative trade-offs between amplifiers. Keep a copy of your write-up so you can compare data with lab9.

To show your understanding of the lab, your write-up should contain:

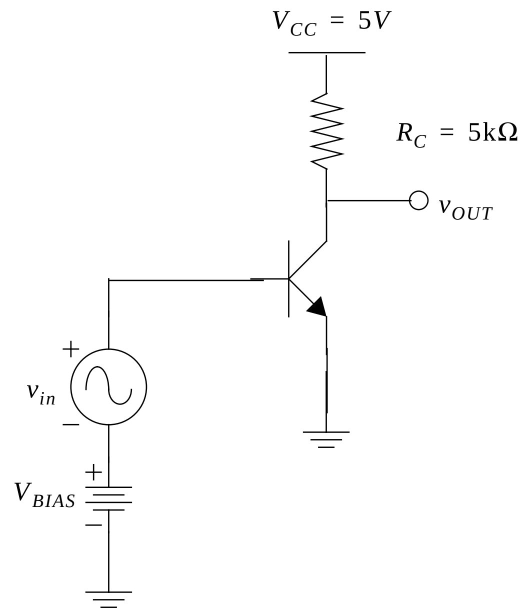
- A table showing the input resistance, output resistance, and gain of the amplifiers
- A discussion on trade-offs issues among the three parameters A_v, R_{in}, and R_{out}
- A discussion explaining the advantages and disadvantages of the different amplifiers

2.0 Prelab

- H & S: Chapters 8.1 - 8.2, 8.7, 8.9
- Biasing will often present a problem when building amplifiers. Below is a npn bipolar transistor which will be configured as a common emitter amplifier. Usually, we would like to have the DC voltage V_{OUT} to be in the middle of the highest and lowest allowable voltage. For the circuit in Fig. 1 below, determine the proper voltage for V_{OUT} (to 2 significant digits) and determine the proper biasing voltage V_{BIAS} needed to achieve this. Use SPICE rather than hand calculations to confirm this. Hand calculations would be useful for a starting point in guessing what V_{BIAS} should be. Use the following parameters:

β_F=100, V_{AF} =100 V, I_S = 1 X 10^{15} A, and $V_{CE(SAT)}$ = 0.2V

FIGURE 1. Bipolar npn Transistor in the Common Emitter Configuration



3.0 Procedure

For all the experiments in this lab, use a 5 kHz sine wave with an amplitude of 200 mV.

Lab Tip

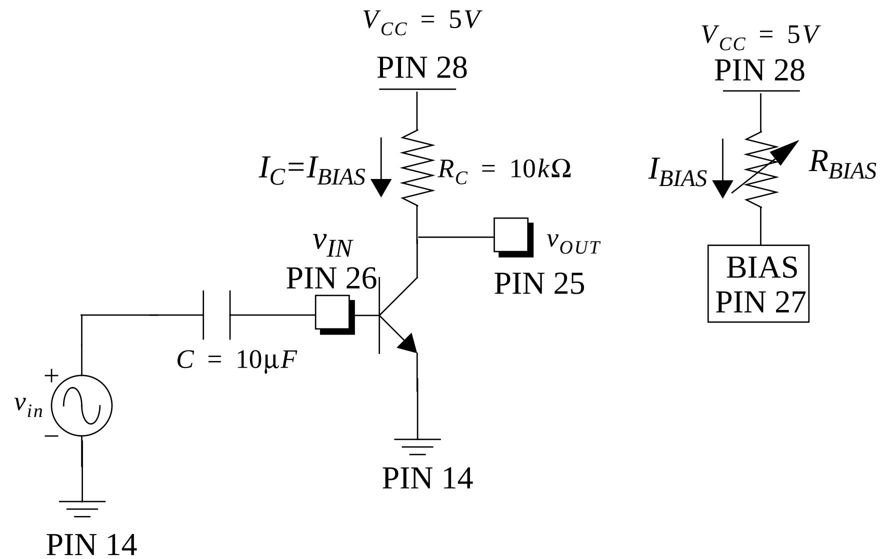
Make sure that both channels of the oscilloscope is calibrated since you will be comparing the signal at the output and comparing it with the input.

Grounding the circuit’s ground to the metal base of the breadboard can give cleaner signals.

Do **not** trigger the oscilloscope in *Vert Mode*. You will lose phase information!

Most of the circuits here will contain special biasing circuits to set the collector currents of the npns or the drain currents of the FETs. The drain or collector currents will be equal to the current across a biasing resistor -- there is an internal circuit that is responsible which we will study in Exp. 11. The circuit below will illustrate this point.

FIGURE 2. Common Emitter with Internal Biasing Circuit on Lab Chip 3



The user will provide R_{BIAS} across pin 28 and pin 27. The current across the resistor, I_{BIAS}, becomes the collector current I_C for the BJT. I_{BIAS} can be found by use of a voltmeter across R_{BIAS}., with I_{BIAS} equal to the voltage across the resistor divided by its resistance.

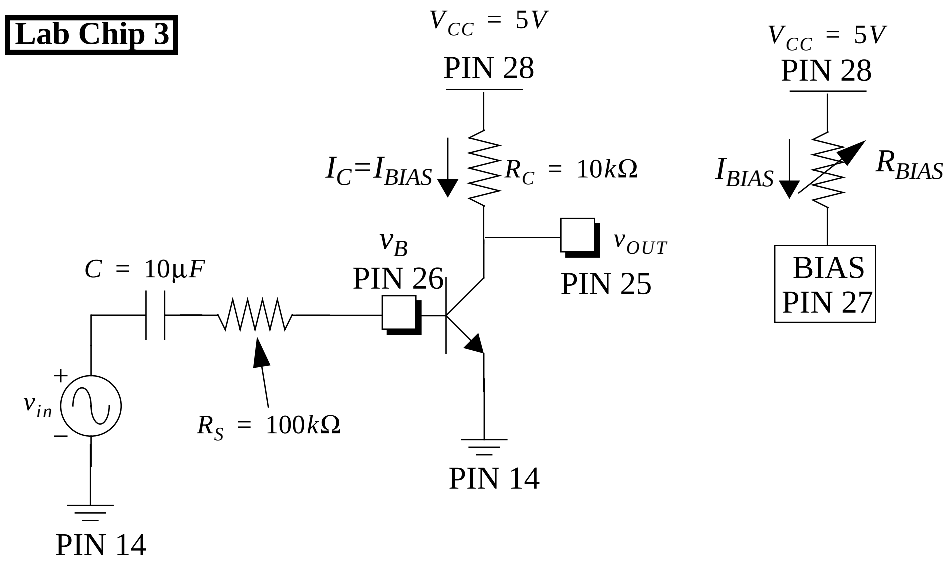
3.1 Common Emitter Amplifier

1. For the circuit in figure 3, adjust R_{BIAS} until V_{OUT} = 2.5V. (R_{BIAS} should be about 16 kΩ) Measure the current through R_{BIAS}. Is it the same as the collector current? Also check V_{BE} and V_{BC} to verify that the transistor is in its forward action region of operation. Why is V_{OUT} = 2.5 V a good choice?
2. Using the oscilloscope, measure the small-signal voltage gains.

$$A_{v1} = \frac{v_{out}}{v_b}$$

$$A_{v2} = \frac{v_{out}}{v_{in}}$$

FIGURE 3. Common Emitter Amplifier with Base Resistor for procedure 3.1



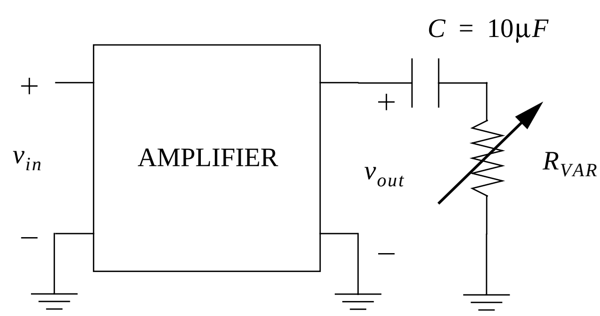
3.1.1 Input Resistance Measurement

1. Why is A_{v2} lower than A_{v1}? What is the relationship if between A_{v2} and A_{v1}? Note that the open-loop voltage gain of the amplifier is A_{v1}, not A_{v2}.
2. Using that relationship, you should be able to find the input resistance. In this case, the input resistance happens to be r_π.What is the value of r_π?

3.1.2 Output Resistance Measurement

1. Measure the amplitude at v_{out}. Connect the capacitor and the variable resistor to the output of the circuit as depicted in figure 4. Adjust the resistance until the amplitude at v_{out} is reduced by one-half. The value of the variable resistor is equal to the output resistance. Explain why this procedure measures the output resistance. Also explain the function of the capacitor.

FIGURE 4. 2-Port Representation of Amplifier to find R_{out}



3.2 Common Collector Amplifier (Emitter Follower)

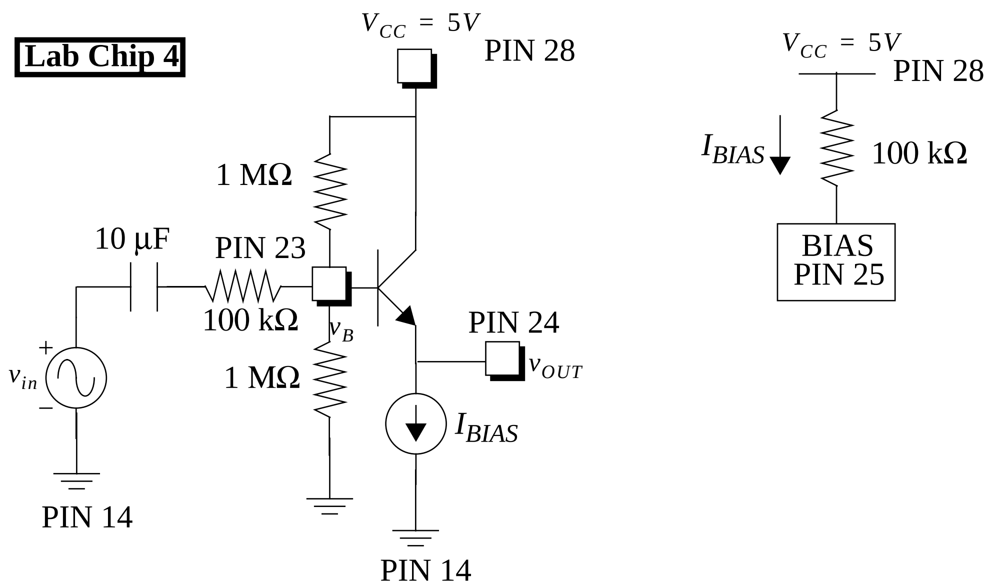
1. Figure 5 shows a common collector circuit with a current source bias. I_{BIAS} is the same current as through R_{BIAS}. Let R_{BIAS} be 100kΩ, I_{BIAS}. What is the voltage gain?

$$A_{v3} = \frac{v_{out}}{v_b}$$

$$A_{v4} = \frac{v_{out}}{v_{in}}$$

2. Find the input and output resistance using the methods from earlier sections. The current source is actually an npn transistor, so its output resistance is just $r_o = V_A/I_C$. Note that the voltage gain of the common collector configuration cannot exceed unity. Do your results agree? In what situation would one use a Common Collector?

FIGURE 5. Common Collector Amplifier with Internal Bias Circuit.



4.0 Optional Experiments

4.1 Common Emitter with Emitter Degeneration

1. Connect the circuit shown in figure 6. Why is there no biasing problem with this circuit? Repeat the procedures for the Common Emitter Amplifier. How do the values of voltage gain, input impedance, and output impedance compare to the corresponding values for the common emitter configuration?

FIGURE 6. Common Emitter with Emitter Degeneration