Experiment 9- Single Stage Amplifiers with Passive Loads - MOS

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1.0 Objective

This is the second part of the single stage amplifier lab. We will be dealing with MOS amplifiers in this experiment.

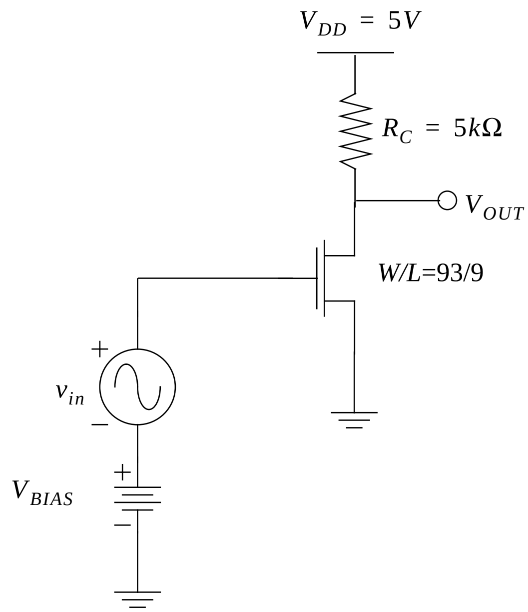
To show your understanding of the lab, your write-up should contain:

- A table showing the input resistance, output resistance, and gain
- A discussion on trade-offs issues among the three parameters A_v, R_{in}, and R_{out}
- A discussion explaining the advantages and disadvantages of the different amplifiers
- A discussion of the differences between similar MOS and BJT amplifier stages

2.0 Prelab

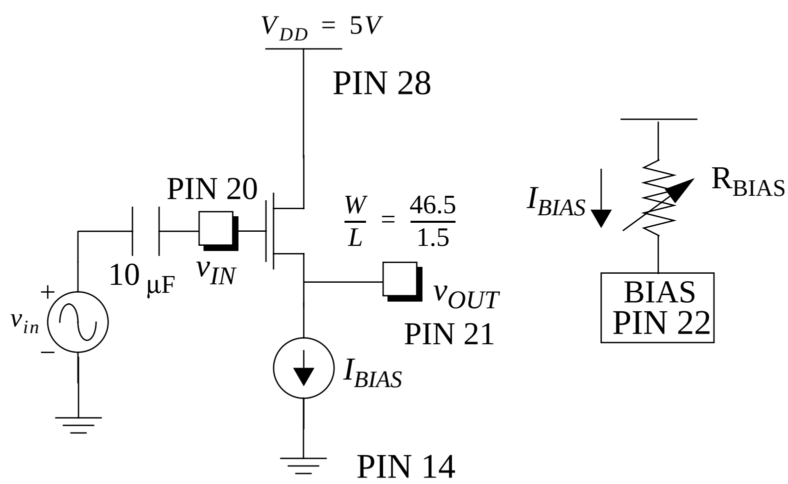
- H&S: Chapter 8.3, 8.9
- You will now consider biasing issues with FETs. Below is an NMOS transistor that will be configured as a Common Source Amplifier. For the figure below, bias the circuit so that V_{OUT} = 2.50 V. Determine the proper bias voltage V_{BIAS} needed to achieve this. What can you say about the value of V_{BIAS} when compared to V_{BIAS} for the common emitter amplifier? Use the following MOS parameters for hand calculation and for SPICE, in which you should plot V_{OUT} vs. V_{BIAS}.
  $V_{TO} = 0.9$ V, $K_p = 20 \times 10^{-6}$ A/V^2, $\lambda = 0.05$ V^{-1}

FIGURE 1. NMOS Transistor in the Common Source Configuration



3.0 Procedure

FIGURE 2. Common Drain with Biasing Circuit (Lab Chip 4 SF = source follower)

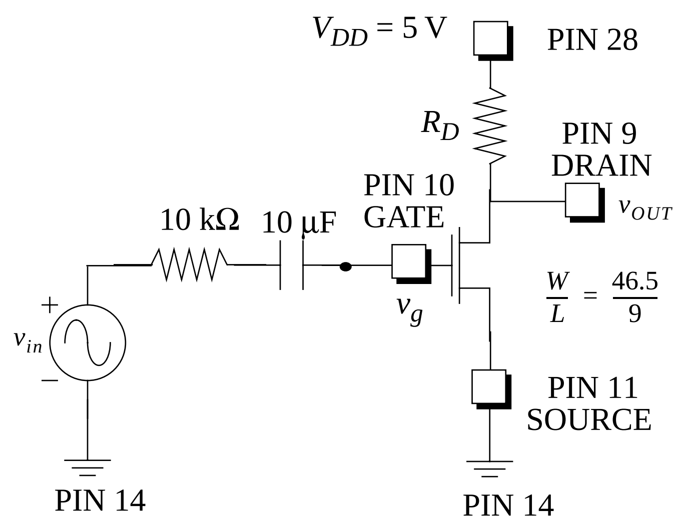


Many of the amplifiers will contain special biasing current sources to set the collector currents of the npns or the drain currents of the FETs. The drain or collector currents will be equal to the current in an external resistor R_{BIAS}. The user provides R_{BIAS} across pin 28 and pin 22. The current through the resistor is equal to I_{BIAS} which sets the I_D for the NMOS transistor. I_{BIAS} can be found by use of a voltmeter across R_{BIAS}.

3.1 Common Source Amplifier

3. Figure 3 shows a Common Source amplifier. Let R_D = 50 kΩ
4. Let v_{in} be a sinusoid with an amplitude of 100 mV at a frequency of 5 kHz.
5. Measure V_{OUT} and verify that the transistor is operating in the constant-current (saturation) region. Measure the value of the drain current and compare it with the calculated value.

FIGURE 3. Common Source Amplifier (Lab Chip 1)

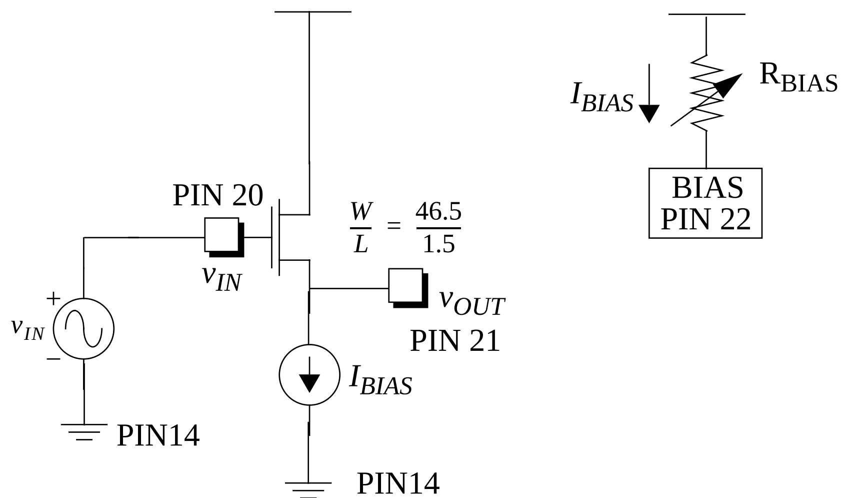


6. Use the oscilloscope to measure the voltage gain v_{out}/v_{in}. Make sure that the output isn't clipping. Also measure v_g/v_{in}. Find the gain. Compare the value of the gain to that of the Common Emitter.
7. One major difference between bipolar and MOS transistors is that the MOS transistor has an infinite input impedance. Because of this high input impedance, there is no voltage attenuation from the voltage source to the amplifier input, even if the voltage source has a large source resistance. Verify that this is true by measuring v_g/v_{in}. You can obtain an estimate of the input resistance of the common source amplifier from the gain v_g/v_{in}.
8. Measure the output impedance using a technique similar to the method used to measure the output impedance of the bipolar amplifiers in Exp. 8.

3.2 Common Drain Amplifier (Source Follower)

1. Figure 4 shows a Common Drain amplifier with a current source biasing. The current source is really an NMOS transistor and its small-signal resistance is $1 / (\lambda_n I_D)$. Its bias current is the current through R_{BIAS} = 10 kΩ. Let v_{IN} be a sinusoid with an amplitude of 200 mV at a frequency of 5 kHz and a DC offset of 3 V. Repeat the steps above to find the gain and output resistance. As with common collectors, common drains are also used as voltage buffers. I_{BIAS} is the same current through R_{BIAS}.

FIGURE 4. Common Drain Amplifier (Lab Chip 4)



4.0 Optional Experiments

4.1 Common Source with Source Degeneration

1. Connect the circuit of figure 9. Let R_D=5 kΩ, R_S=500 Ω, and V_{BIAS}=3 V. Find the gain, input resistance and output resistance. Note: V_{Tn} will not equal V_{TOn} because of the backgate effect. Source degeneration in MOS amplifier stages is not as widely used as emitter degeneration in bipolar circuits. The transconductance of MOS transistors is much lower than that of bipolar transistors so that further reduction in g_m is usually undesirable. Also, the beneficial effect of raising the input impedance of a bipolar transistor is irrelevant for MOS transistors since the input impedance is infinite. Degeneration is occasionally useful for making the transconductance independent of the device characteristics.

FIGURE 5. Common Source with Source Degeneration (Lab Chip 1, NMOS2)