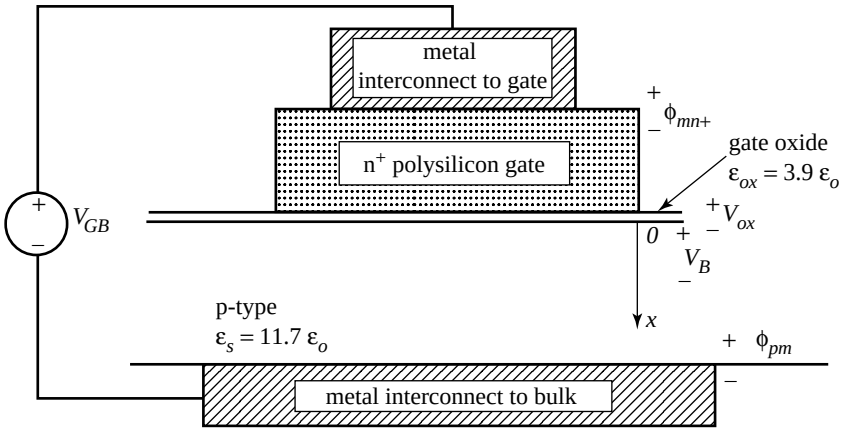
MOS Capacitor under Applied Bias

- Oxide doesn't permit any steady-state current between the n^+ poly gate and the substrate. Therefore, if we wait long enough for transient currents to die out, the electron and hole currents are zero --

$$J_n = 0 \quad \text{and} \quad J_p = 0$$

- Even though the structure isn't in equilibrium, the absence of current implies that we can relate potential to carrier concentration in the silicon substrate (since that's all we assumed in deriving the 60 mV rule.)

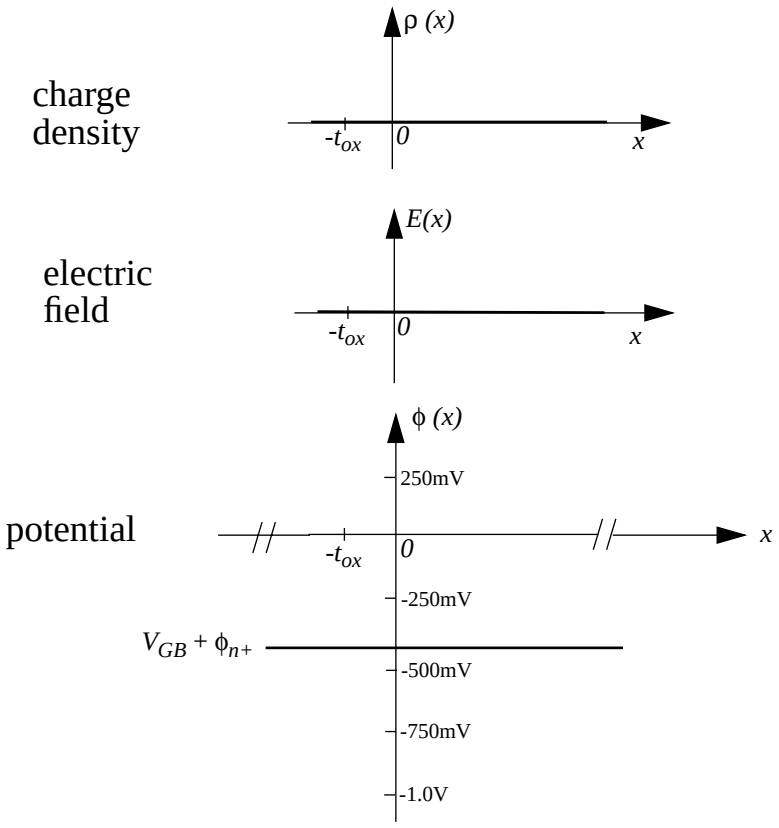


- Flatband condition: cancel built-in drop by applying the *flatband voltage*

$$V_{GB} = -(\phi_{n+} - \phi_p) = V_{FB} = -970 \text{ mV for } N_a = 10^{17} \text{ cm}^{-3}$$

MOS Electrostatics in Flatband

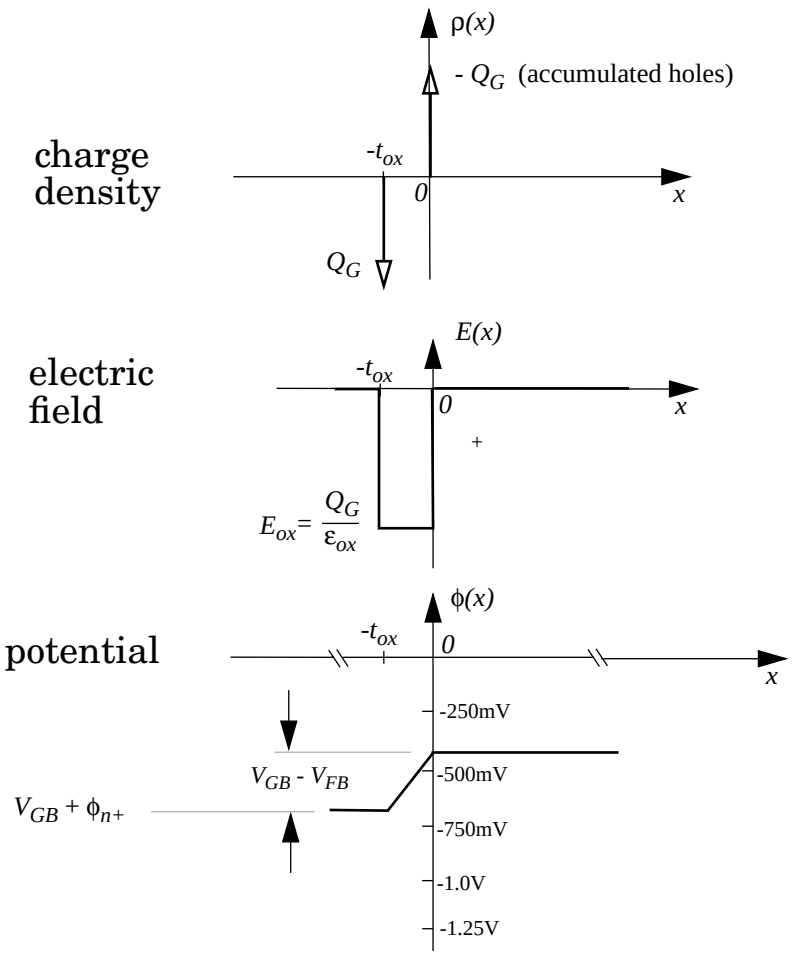
- When $V_{GB} = V_{FB}$, the gate is shifted from its thermal equilibrium potential (ϕ_{n+}) to a new value of $V_{FB} + \phi_{n+} = -(\phi_{n+} - \phi_p) + \phi_{n+} = \phi_p$, which is the same potential as the p-type bulk. Therefore, there is no potential drop across the MOS structure in flatband



- If we continue to make the gate-bulk voltage more negative, the gate will take on a negative charge $Q_G < 0$. The substrate has a positive charge, which comes from holes that are attracted by the negative gate charge

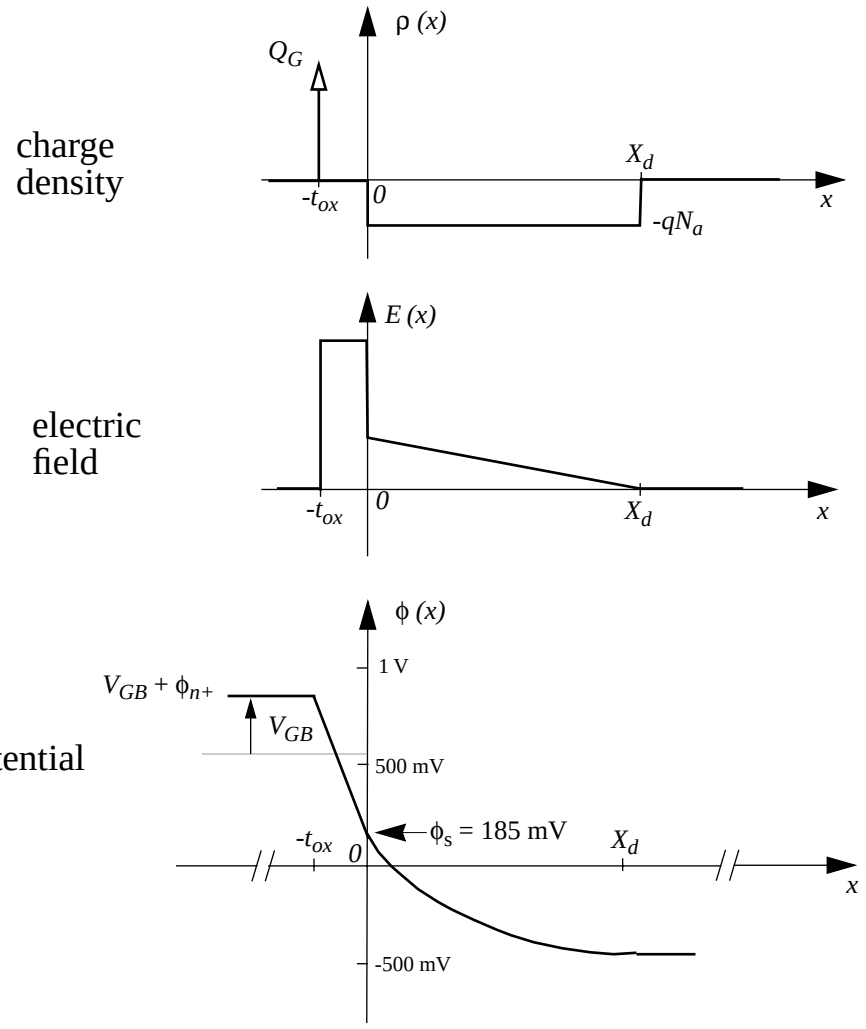
MOS Capacitor in Accumulation

- Charge density, electric field, and potential in accumulation: $V_{GB} < V_{FB}$, where V_{FB} = - 0.97 V for this example.



MOS Capacitor in Depletion

- Now we make $V_{GB} > V_{FB}$. Note that thermal equilibrium falls into this range of applied bias.



- Surface potential at oxide/silicon interface is now positive --> n-type (slightly, $n_s = 10^{13}$ cm^{-3}).

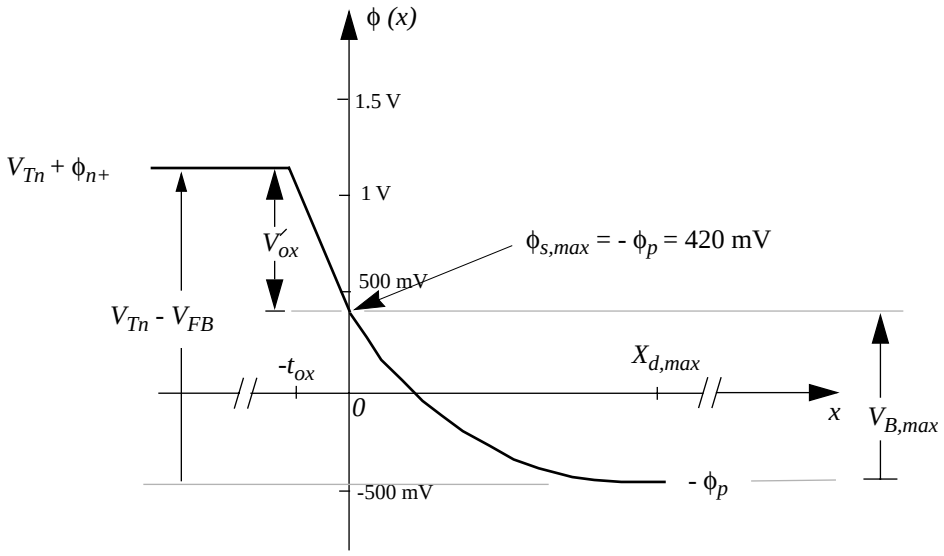
The Threshold Voltage V_{Tn}

- Keep increasing V_{GB} --> surface potential keeps increasing. At some point, the surface is n-type (i.e., we say that it is *inverted*) and the electron charge makes a significant contribution to the charge density.

  How do we model this phenomenon? We approximate that onset of inversion as the point where the electron concentration n_s at the surface is the same as the hole concentration N_a in the bulk. (In other words, "the surface is as n-type as the bulk is p-type.")

  The gate-bulk potential at the onset of inversion is called the *threshold voltage*, V_{Tn}. To find the threshold voltage, we need to consider the electrostatics in depletion (no electrons at the surface at the onset of inversion) -- with the surface potential equal to the opposite of the bulk potential:

$$\phi_{s,\,max} = -\phi_p$$



Threshold Voltage Expression

- We can solve for the threshold voltage:

$$V_T - V_{FB} = V_{ox}' + V_{B,\,max}$$

- The drop across the depletion region is

$$V_{B,\,max} = \phi_{s,\,max} - \phi_p = -\phi_p - \phi_p = -2\phi_p$$

- The drop across the oxide for $V_{GB} = V_{Tn}$ is

$$V_{ox}' = E_{ox}' t_{ox} = \left(\frac{-Q_{B,\,max}}{\varepsilon_{ox}}\right) t_{ox} = \frac{-Q_{B,\,max}}{C_{ox}}$$

- The bulk charge in inversion is found from the depletion width $X_{d,max}$

$$Q_{B,\,max} = -qN_a X_{d,\,max} = -qN_a \sqrt{\frac{-2\phi_p}{((1/2)qN_a)/\varepsilon_s}} = -\sqrt{2q\varepsilon_s N_a(-2\phi_p)}$$

where the relationship between the depletion width $X_{d,max}$ and the drop across the depletion region $\phi_{s,max}$ - (ϕ_p) = -ϕ_p - ϕ_p = -2ϕ_p can be found from Poisson's Equation.

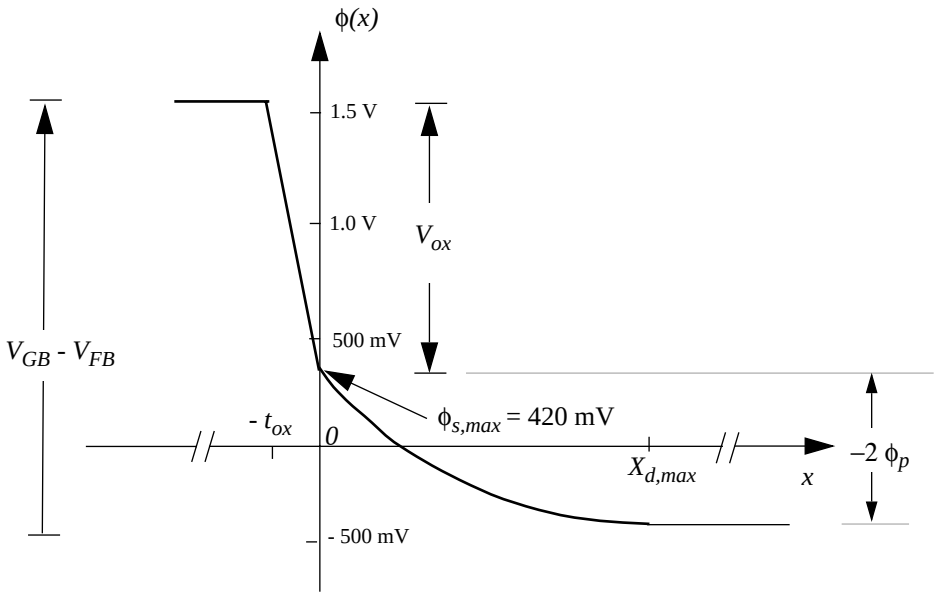
Threshold Voltage (p-type Substrate)

- The threshold voltage is the sum of the flatband voltage (which cancels the built-in potential drop from gate to bulk), the drop across the oxide at the onset of inversion, and the maximum potential drop across the depletion region

$$V_{Tn} = V_{FB} - 2\phi_p + \frac{1}{C_{ox}}\sqrt{2q\varepsilon_s N_a(-2\phi_p)}$$

The Inverted MOS Capacitor ($V_{GB} > V_{Tn}$)

- We consider the surface potential as fixed ("pinned") at $\phi_{s,max} = -2\,\phi_p$



- What is the inversion charge Q_N?

  see Section 3.7 for the derivation

  consider: bulk charge is constant for $V_{GB} > V_{Tn}$ --> all of the additional charge in the silicon is stored in the inversion layer, once inversion occurs. The inversion layer is separated from the gate by the gate oxide; we can relate the inversion charge (per cm^2) to the applied voltage over V_{Tn} through C_{ox} the capacitance (per cm^2) of the oxide

$$Q_N = -C_{ox}(V_{GB} - V_{Tn})$$

Charge Storage in the MOS Structure

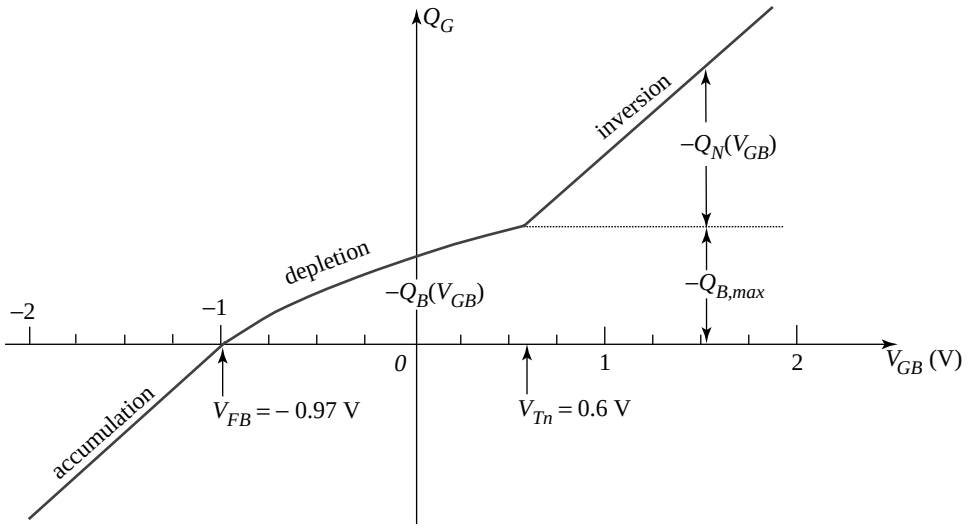
- Three regions of operation:

  Accumulation: $q_G = C_{ox}\,(v_{GB} - v_{FB})$ ... parallel plate capacitor

  Depletion: $q_G = -\,q_B(v_{GB})$, with the bulk (depletion) charge in the silicon being a nonlinear function of v_{GB}

  Inversion: $q_G = -\,q_N - q_{B,max}$, where $q_{B,max} = q_B(v_{GB} = V_T)$ is the depletion charge at the onset of inversion and

- Sketch of the gate charge as a function of gate-bulk voltage:

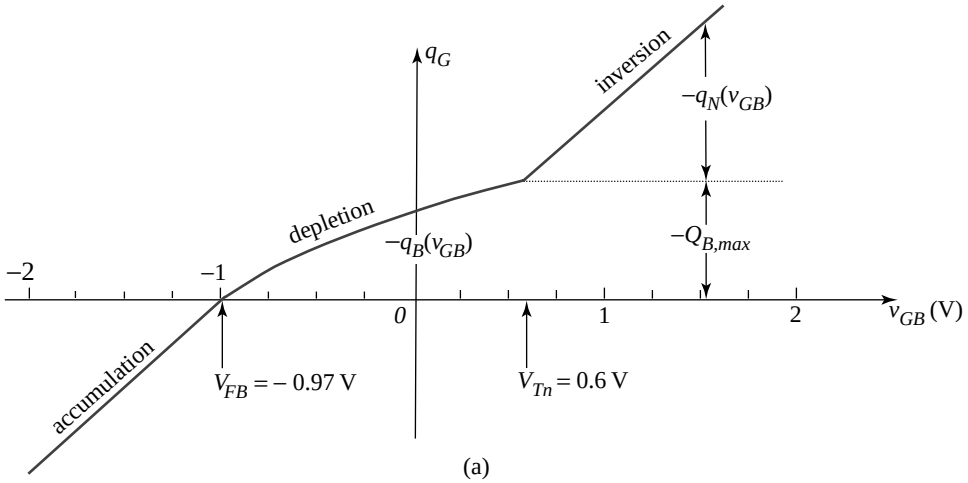


MOS Capacitance

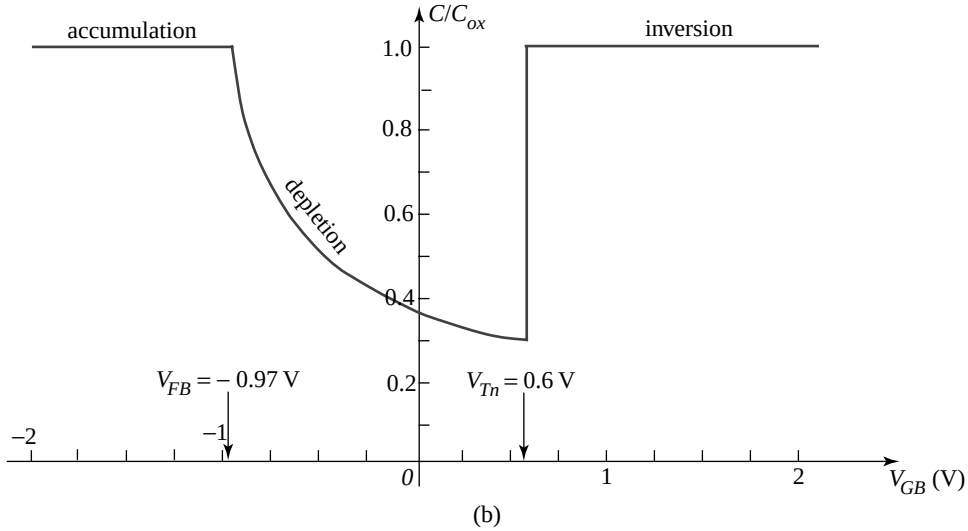
- The capacitance of the MOS structure is defined as

$$C = \left.\frac{dq_G}{dv_{GB}}\right|_{V_{GB}}$$

- From sketch, determine the slope and plot as the capacitance



(a)

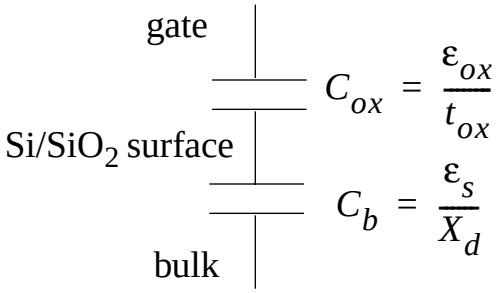


(b)

Physical Interpretation of MOS Capacitance

- ***Accumulation***: parallel plate capacitor --> $C = C_{ox}$

- ***Depletion***: increment in gate charge is mirrored at bottom of depletion region, so capacitance model is C_{ox} in series with the depletion region capacitance C_b



$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

$$C_b = \frac{\varepsilon_s}{X_d}$$

Note that X_d is a function of V_{GB}

$$C = C_{ox} \| C_b$$

- ***Inversion***: bulk charge is no longer changing with V_{GB} --> an increment in gate charge is mirrored in the inversion layer under the gate.

  The capacitance is therefore the same as in accumulation --> $C = C_{ox}$

Understanding MOS Capacitors

- **Step 1**: identify the flatband voltage from the gate and bulk potentials in equilibrium
- **Step 2**: determine whether $V_{GB} > V_{FB}$ leads to *accumulation* or to *depletion*

  substrate is n-type --> accumulation substrate is p-type --> depletion

  Why? positive charge on gate (since $V_{GB} - V_{FB} > 0$ V) *must* be mirrored by a *negative* charge in the substrate.

  n-type substrate: negatively charged electrons are accumulated under the gate
  p-type substrate: negatively charged ionized acceptors are left, after holes are repelled away from positive charge on gate
- **Step 3**: construct $C(V_{GB})$ plot, using the knowledge that the substrate is depleted on the other side of V_{FB} from accumulation in Step 2 and that *inversion* occurs after depletion. Calculation of V_T and C_{min} is necessary to quantify the plot
- Additional data point: determine state of MOS structure in thermal equilibrium ($V_{GB} = 0$ V) ... accumulation or [depletion/inversion]

Example:

gate: p^+ polysilicon (where $\phi_{p+} = -550$ mV); gate oxide thickness = 200 Å ,
substrate: n type silicon, $\phi_n = 480$ mV ($N_d = 10^{18}$ cm^{-3})

$V_{FB} = -(-550 \text{ mV} - 480 \text{ mV}) = +1.03$ V

$V_{GB} - V_{FB} > 0$ V --> accumulated; substrate is depleted for $V_{GB} < 1.03$ V

Check: $V_{GB} = 0$ --> negative charge on gate; positive in bulk (since gate is at - 0.55 V and substrate is at + 0.48 V in thermal equilibrium) --> positive donors in depletion region under gate ... and possibly holes due to inversion

MOS Capacitance-Voltage Curve

- Evaluate threshold voltage V_{Tp}

$$V_{Tp} = V_{FB} - 2\phi_n - \frac{\sqrt{2q\varepsilon_s N_d (2\phi_n)}}{C_{ox}} = 1.03 - 2(0.48) - 3.28 = -3.21 \text{ V}$$

- Minimum capacitance occurs just prior to inversion and is the series combination of the oxide capacitance and the maximum depletion capacitance:

$$C_{min} = \left(\frac{\varepsilon_{ox}}{t_{ox}}\right) \Bigg\| \left(\frac{\varepsilon_s}{X_{d,\,max}}\right) = \left(\frac{3.45\times10^{-13}}{2\times10^{-6}}\right) \Bigg\| \left(\frac{1.04\times10^{-12}}{2.9\times10^{-6}}\right) = 1.16 \text{ fF/cm}^2$$

- Maximum capacitance is C_{ox} = 1.72 fF/cm^2.