p-channel MOSFET Models

- DC drain current in the three operating regions: \(-I_D > 0\)

\[-I_D = 0 \text{ A} \] \hspace{1cm} (\(V_{SG} \leq -V_T\))
\[-I_D = \mu_p C_{ox}(W/L)(V_{SG} + V_{T_p} - (V_{SD}/2))(1 + \lambda_p V_{SD})V_{SD} \] \hspace{1cm} (\(V_{SG} \geq -V_{T_p}, V_{SD} \leq V_{SG} + V_{T_p}\))
\[-I_D = \mu_p C_{ox}(W/(2L))(V_{SG} + V_{T_p})^2(1 + \lambda_p V_{SD}) \] \hspace{1cm} (\(V_{SG} \geq -V_{T_p}, V_{SD} \geq V_{SG} + V_{T_p}\))

- The threshold voltage with backgate effect is given by:

\[V_{T_p} = V_{TOp} - \gamma_p ((\sqrt{-V_{SB} + 2\phi_n}) - (2\phi_n))\]

**Numerical values:**

\(\mu_p C_{ox}\) is a measured parameter. Typical value: \(\mu_p C_{ox} = 25 \mu\text{AV}^{-2}\)

\[\lambda_p \approx \frac{0.1\mu\text{mV}^{-1}}{L}\]

\(V_{T_p} = -0.7\) to \(-1.0\) V, which should be approximately \(-V_{T_n}\) for a well-controlled CMOS process
MOSFET Small-Signal Model

- Concept: find an equivalent circuit which interrelates the incremental changes in $i_D$, $v_{GS}$, $v_{DS}$, etc. Since the changes are small, the small-signal equivalent circuit has linear elements only (e.g., capacitors, resistors, controlled sources).

- Derivation: consider for example the relationship of the increment in drain current due to an increment in gate-source voltage when the MOSFET is saturated—with all other voltages held constant.

\[ v_{GS} = V_{GS} + v_{gs}, \ i_D = I_D + i_d -- \text{we want to find } i_d = (\ ?) v_{gs} \]

We have the functional dependence of the total drain current in saturation:

\[ i_D = \mu_n C_{ox} \left( \frac{W}{2L} \right) (v_{GS} - V_{Th})^2 (1 + \lambda_n v_{DS}) = i_D(v_{GS}, v_{DS}, v_{BS}) \]

Do a Taylor expansion around the DC operating point (also called the quiescent point or $Q$ point) defined by the DC voltages $Q(V_{GS}, V_{DS}, V_{BS})$:

\[ i_D = I_D + \left. \frac{\partial i_D}{\partial v_{GS}} \right|_Q (v_{gs}) + \left. \frac{1}{2} \frac{\partial^2 i_D}{\partial v_{GS}^2} \right|_Q (v_{gs})^2 + \ldots \]

If the small-signal voltage is really “small,” then we can neglect all everything past the linear term --

\[ i_D = I_D + \left. \frac{\partial i_D}{\partial v_{GS}} \right|_Q (v_{gs}) = I_D + g_m v_{gs} \]

where the partial derivative is defined as the transconductance, $g_m$. 
Transconductance

The small-signal drain current due to $v_{gs}$ is therefore given by

$$i_d = g_m v_{gs}.$$
Another View of $g_m$

* Plot the drain current as a function of the gate-source voltage, so that the slope can be identified with the transconductance:
Transconductance (cont.)

- Evaluating the partial derivative:

\[ g_m = \mu_n C_{ox} \left( \frac{W}{L} \right) (V_{GS} - V_{Tn}) (1 + \lambda_n V_{DS}) \]

Note that the transconductance is a function of the operating point, through its dependence on \( V_{GS} \) and \( V_{DS} \) -- and also the dependence of the threshold voltage on the backgate bias \( V_{BS} \).

- In order to find a simple expression that highlights the dependence of \( g_m \) on the DC drain current, we neglect the (usually) small error in writing:

\[ g_m = \sqrt{2\mu_n C_{ox} \left( \frac{W}{L} \right) I_D} = \frac{2I_D}{V_{GS} - V_{Tn}} \]

For typical values \((W/L) = 10, I_D = 100 \text{ mA}, \) and \( \mu_n C_{ox} = 50 \text{ mAV}^{-2} \) we find that \( g_m = 320 \text{ mAV}^{-1} = 0.32 \text{ mS} \)

- How do we make a circuit which expresses \( i_d = g_m v_{gs} \)? Since the current is not across the controlling voltage, we need a voltage-controlled current source:

![Circuit diagram](image-url)
Output Conductance

- We can also find the change in drain current due to an increment in the drain-source voltage:

\[
g_o = \frac{\partial i_D}{\partial v_{DS}} \bigg|_Q = \frac{\partial i_D}{\partial v_{DS}} = \mu_n C_{ox} \left( \frac{W}{2L} \right) (V_{GS} - V_T)^2 \lambda_n \equiv \lambda_n I_D
\]

The output resistance is the inverse of the output conductance

\[
r_o = \frac{1}{g_o} = \frac{1}{\lambda_n I_D}
\]

The small-signal circuit model with \( r_o \) added looks like:

\[
i_d = g_m v_{gs} + (1/r_o)v_{ds}
\]
Backgate Transconductance

We can find the small-signal drain current due to a change in the backgate bias by the same technique. The chain rule comes in handy to make use of our previous result for $g_m$:

\[
g_{mb} = \frac{\partial i_D}{\partial v_{BS}} = \frac{\partial i_D}{\partial V_T} \frac{\partial V_T}{\partial v_{BS}} = \left( -g_m \right) \frac{\partial V_T}{\partial v_{BS}} = \left( -g_m \right) \left( -\frac{\gamma}{2\sqrt{-2\phi_p-V_{BS}}} \right) = \frac{\gamma_n g_m}{2\sqrt{-2\phi_p-V_{BS}}}.
\]

The ratio of the “front-gate” transconductance $g_m$ to the backgate transconductance $g_{mb}$ is:

\[
\frac{g_{mb}}{g_m} = \frac{\sqrt{2q\varepsilon_s N_a}}{2C_{ox}\sqrt{-2\phi_p-V_{BS}}} = \frac{1}{C_{ox}} \frac{\sqrt{q\varepsilon_s N_a}}{2(-2\phi_p-V_{BS})} = \frac{C_b(y=0)}{C_{ox}}
\]

where $C_b(y=0)$ is the depletion capacitance at the source end of the channel --
In saturation, the gate-source capacitance contains two terms, one due to the channel charge’s dependence on $v_{GS}$ \((2/3)WLC_{ox}\) and one due to the overlap of gate and source \((WC_{ov}\) where $C_{ov}$ is the overlap capacitance in fF per µm of gate width) 

\[
C_{gs} = \frac{2}{3} WLC_{ox} + WC_{ov}
\]

In addition, there are depletion capacitances between the drain and bulk \((C_{db})\) and between source and bulk \((C_{sb})\). Finally, the extension of the gate over the field oxide leads to a small gate-bulk capacitance \(C_{gb}\).
Complete Small-Signal Model

- The capacitances are “patched” onto the small-signal circuit schematic containing $g_m$, $g_{mb}$, and $r_o$

- p-channel MOSFET small-signal model

  the source is the highest potential and is located at the top of the schematic
Circuit Simulation

■ **Objectives:**
  
  • fabricating an IC costs $1000 ... $100,000 per run
      ---> nice to get it “right” the first time
  
  • check results from hand-analysis
      (e.g. validity of assumptions)
  
  • evaluate functionality, speed, accuracy, ... of large circuit blocks or entire chips

■ **Simulators:**
  
  • **SPICE:** invented at UC Berkeley circa 1970-1975
      commercial versions: HSPICE, PSPICE, I-SPICE, ... (same core as Berkeley SPICE, but add functionality, improved user interface, ...)
      EE 105: student version of PSPICE on PC, limited to 10 transistors
  
  • other simulators for higher speed, special needs (e.g. SPLICE, RSIM)

■ **Limitations:**
  
  • simulation results provide no insight (e.g. how to increase speed of circuit)
  
  • results sometimes wrong (errors in input, effect not modeled in SPICE)

  ===> always do hand-analysis first and COMPARE RESULTS
MOSFET Geometry in SPICE

- Statement for MOSFET ... $D, G, S, B$ are node numbers for drain, gate, source, and bulk terminals

$$M_{\text{name}} \, D \, G \, S \, B \, MOD_{\text{name}} \, L=\_ \, W=\_ \, AD=\_ \, AS=\_ \, PD=\_ \, PS=\_$$

$MOD_{\text{name}}$ specifies the model name for the MOSFET

![Diagram of MOSFET geometry with labels and equations](image)
MOSFET Model Statement

```
.MODMODEL MODname NMOS/PMOS VTO= KP= GAMMA= PHI=
LAMBDA= RD= RS= RSH= CBD= CBS= CJ= MJ= CJSW=
MJSW= PB= IS= CGDO= CGSO= CGBO= TOX= LD=
```

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<th>Analytical symbol Eqs. (4.93), (4.94)</th>
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<td>surface potential/depletion drop in inversion</td>
<td>$PHI$</td>
<td>$-\phi_p$</td>
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DC Drain Current Equations:

\[
I_{DS} = 0 \quad (V_{GS} \leq -V_{TH})
\]

\[
I_{DS} = \frac{KP}{2} (W/L_{eff}) V_{DS} [2(V_{GS} - V_{TH}) - V_{DS}] (1 + LAMBDA \cdot V_{DS}) \quad (0 \leq V_{DS} \leq V_{GS} - V_{TH})
\]

\[
I_{DS} = \frac{KP}{2} (W/L_{eff}) (V_{GS} - V_{TH})^2 (1 + LAMBDA \cdot V_{DS}) \quad (0 \leq V_{GS} - V_{TH} \leq V_{DS})
\]

\[
V_{TH} = V_{TO} + GAMMA(\sqrt{\frac{2}{3} \cdot PHI} - V_{BS} - \sqrt{\frac{2}{3} \cdot PHI})
\]
Capacitances

SPICE includes the “sidewall” capacitance due to the perimeter of the source and drain junctions --

\[
C_{BD}(V_{BD}) = \frac{CJ \cdot AD}{(1 - V_{BD}/PB)^{MJ}} + \frac{CJSW \cdot PD}{(1 - V_{BD}/PB)^{MJSW}}
\]

Gate-source and gate-bulk overlap capacitance are specified by \( CGDO \) and \( CGSO \) (units: F/m).

Level 1 MOSFET model:

```
.MODEL MODN NMOS LEVEL=1 VTO=1 KP=50U LAMBDA=.033 GAMMA=.6
+ PHI=0.8 TOX=1.5E-10 CGDO=5E-10 CGSO= 5e-10 CJ=1E-4 CJSW=5E-10
+ MJ=0.5 PB=0.95
```

The Level 1 model is adequate for channel lengths longer than about 1.5 \( \mu \)m

For sub-\( \mu \)m MOSFETs, BSIM = “Berkeley Short-Channel IGFET Model” is the industry-standard SPICE model.